

Integration of through-wafer interconnects with a two-dimensional cantilever array

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Abstract

High-density through-wafer interconnects are incorporated in a two-dimensional (2D) micromachined cantilever array. The design addresses alignment and density issues associated with 2D arrays. Each cantilever has piezoresistive deflection sensors and high-aspect ratio silicon tips. The fabrication process and array operation are described. The integration of cantilevers, tips, and interconnects enables operation of a high-density 2D scanning probe array over large areas. © 2000 Elsevier Science S.A. All rights reserved.

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1. Introduction

The ability to fabricate small through-wafer electrical interconnections has broad applications for integrated circuits and micromachined devices. Semiconductor micro-fabrication generally places sensors and integrated circuits on only one side of a silicon wafer. With bulk wafer etching techniques, connections between both sides of the wafer can be made, enabling more complicated and compact structures. Some of the many examples include interconnects in integrated circuits, three-dimensional (3D) packaging (e.g., stacking), and fabrication of 3D electrical and MEMS structures [1–6]. Small through-wafer interconnects particularly benefit dense arrays of microfabricated sensors, such as ultrasound transducer arrays for imaging and diode arrays for detecting charged particles and X-rays, as they minimize nonsensing area and thus enhance performance [7,8]. In this work, we focus on a

versatile and useful sensor format: two-dimensional (2D) arrays of force sensing cantilevers.

Scanning probe devices, such as an atomic force microscope (AFM), take advantage of high spatial resolution and high force resolution to make significant contributions in a variety of fields. The commercially available AFM can typically measure piconewtons of force, with angstrom vertical resolution and nanometer horizontal resolution. Its ability to operate in water and at atmospheric pressures, unlike scanning electron microscopes (SEM), has led to numerous biological imaging and force measurement applications [9,10]. In lithography, arguably the most critical technology for the integrated circuit industry, scanning probes have demonstrated 300-Å resolution, with a wider process latitude than electron beam techniques [11]. Metal-oxide semiconductor transistors with 100-nm gate lengths have been demonstrated using scanning probe lithography [12]. Scanning probe devices using localized heating can achieve 400 Gbits/in.² data storage densities; an order of magnitude greater than the paramagnetic limit which ultimately limits magnetic data storage [13]. While the sensitivity of these techniques is most impressive, throughput and sensing area are hindered by their reliance on serial scanning. The ability to fabricate large, densely packed, 2D arrays of sensors would address this problem,

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as arrays increase signal throughput without sacrificing the spatial sensitivity of the individual sensor.

One important issue for 2D arrays of scanning probes is alignment. Linear (1D) cantilever probe arrays have been demonstrated for cantilevers operating at a nominal 15° angle relative to the sample surface [14,15]. This arrangement allows access to wire bonds on the tip side of the wafer without interfering with tip to sample alignment (Fig. 1a). Two-dimensional arrays of AFM cantilevers require parallel planar alignment to the sample, so that all cantilevers are simultaneously in contact for scanning (Fig. 1b). In previous 2D cantilever arrays, bond pads with the associated wiring were on the same side of the wafer as the tips [16,17]. This method only works for samples with smaller areas than the cantilever chip. When the sample region is larger than the cantilever array die, wire bonds on the tip side of the wafer would meet the surface before the tips, preventing the ability to scan.

Another challenge for cantilever arrays is the packing density. Increasing the probe density will minimize the imaging time. The electrical wiring for large numbers of devices consumes valuable space, particularly when multiple electrical leads per device are required. When imaging with piezoresistive scanning probes, each cantilever has a deflection lead and a ground connection. High-speed imaging with integrated force feedback additionally requires an individual actuator and its corresponding electrical connections [18]. Similarly, lithography with multiple cantilevers in parallel requires an additional electrical connection for each cantilever to control the exposure dose [19]. Complicated electrical routing on the sensor side of the wafer can be moved to the backside of the wafer by using through-wafer vias (TWVs). Wet etching has been used for through-wafer interconnects, but these techniques leave a hole in one side of the wafer about 0.5 mm^2 in area [3–6]. For dense array applications, this limits ultimate packing

density and layout flexibility. Furthermore, lithography over such 3D topography typically requires electrodeposited resist or shadow masking, which complicate process integration.

In this work, these problems are addressed through the integration of small TWV with a 2D cantilever array. Our previously demonstrated TWVs are used to connect the deflection sensing piezoresistors on the tip side of the wafer with the bond pads on the backside [20]. With the wire bonds on the backside of the wafer, the array is versatile, and can be used to scan samples with a wide range of sizes, similar to commercial AFMs. In addition, highly anisotropic high-density plasma (HDP) etching has enabled these TWVs to be $30 \mu\text{m}$ on a side, an order of magnitude smaller than typically achieved with wet etching [21]. Conventional spin-on resist is used to pattern the TWV thin films, facilitating process integration. The small TWV, combined with an HDP release of the cantilevers, significantly increases the ultimate packing density, and thus the cantilever array throughput.

2. Fabrication

The fabrication process involves three major steps: (1) high-aspect ratio silicon tips, (2) through-wafer interconnects to the piezoresistive sensors, and (3) anisotropic dry release of cantilevers.

The starting substrate is a silicon-on-insulator wafer with a $20\text{-}\mu\text{m}$ silicon device layer and $2\text{-}\mu\text{m}$ buried oxide on a $400\text{-}\mu\text{m}$ silicon handle wafer. High-aspect ratio tips are formed in the device layer silicon in a multistep etch process, similar to previous work [22–25]. First an isotropic plasma etch (SF_6) is used to undercut a silicon dioxide tip mask. Then an anisotropic plasma etch (Cl_2/HBr) is used to control the height of the tip, allowing the flexibility to vary the cantilever thickness. The oxide mask is then removed in buffered hydrofluoric acid (BHF). The tips are sharpened through another isotropic plasma etch (SF_6) followed by a long oxidation to sharpen the tips [26]. Another BHF dip is used to strip the oxide. To form the piezoresistors, a resist pattern is used to mask boron implantations at 40 keV with a dose of $5 \times 10^{14} \text{ cm}^{-2}$. These parameters place the majority of the dopants near the surface of the cantilever, increasing deflection sensitivity [27]. To insure ohmic contacts to the piezoresistors, a heavy implant at 80 keV and $5 \times 10^{15} \text{ cm}^{-2}$ is performed at the base of the piezoresistors where the contact pads will be located (Fig. 2a).

The TWV is made by anisotropically etching $30 \mu\text{m}$ square vias through the entire thickness of the wafer using an HDP etch (SF_6) [21]. The first part of this etch is done from the front of the wafer, through the silicon device layer. The buried oxide is then etched in BHF. The

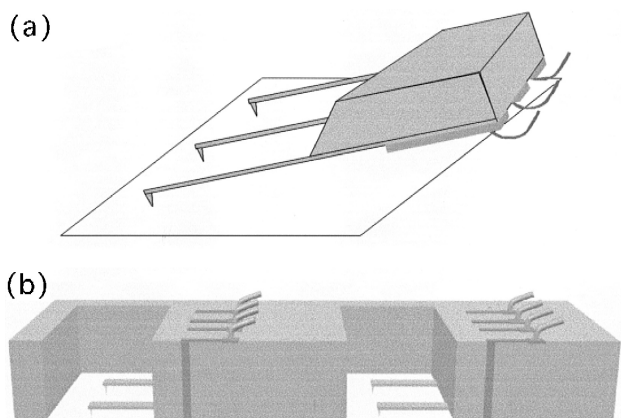


Fig. 1. (a) Linear arrays are operated at an angle with respect to the sample. (b) Two-dimensional arrays must be operated parallel to the sample. Through-wafer interconnects permit wire bonding from the backside of the wafer, facilitating alignment.

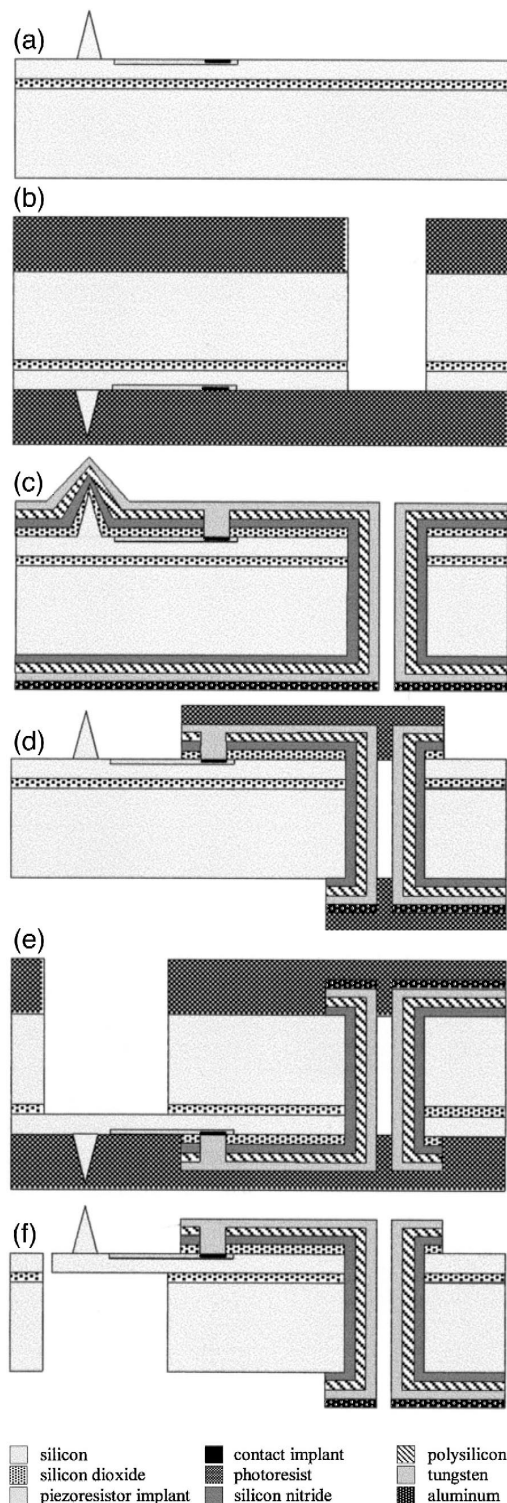


Fig. 2. Process flow for a two-dimensional array of piezoresistive cantilevers with integrated through-wafer electrical interconnects. (a) A high-aspect ratio tip is etched and implants are performed for the piezoresistors and their contacts. (b) The through-wafer via (TWV) is etched. (c) Silicon oxide, silicon nitride, and polysilicon are conformally deposited and then patterned over the piezoresistor contacts. Tungsten is deposited as the metal layer through the TWV, followed by aluminum on the back for wire bonding. (d) The frontside and backside metal are patterned. (e) The cantilever is released from the back with a deep silicon and oxide etch. (f) Resist is removed for the final release of the cantilever.

majority of the TWV is etched from the back of the wafer (4 h etch) with another resist mask, which is aligned to the front side using a backside aligner (Fig. 2b). Etching from the front side first followed by the backside serves to simplify buried oxide removal (easier to wet from the top) and simplifies tip protection (tips do not experience a long plasma etch). Hereafter, simple spin-on resist masks were used repeatedly to protect the bottom-side of the wafer, facilitating double-sided wafer processing.

Multiple thin films are then deposited to form the through-wafer interconnect. A half-micron of low-pressure chemical vapor deposition (LPCVD) oxide is deposited to serve as a future etch-stop for protecting the silicon tips. Conformal LPCVD silicon nitride ($1\ \mu\text{m}$) is used for via electrical isolation, followed by LPCVD polysilicon ($1\ \mu\text{m}$) for tungsten adhesion. Contacts to the piezoresistors are patterned and CVD tungsten ($1\ \mu\text{m}$) is deposited. Aluminum is sputtered on the backside to aid wire bonding, as tungsten does not adhere well to aluminum or gold bond wires (Fig. 2c). Unlike our previous through-wafer interconnect work which used electrodeposited resist, patterning of the front and back metal is done with conventional spin-on thick photoresist (Shipley AZ4620) [2,20]. If spun-on thick ($15\text{--}20\ \mu\text{m}$) and baked resist-side down in a convection oven (90°C for 1 h), the resist is able to harden

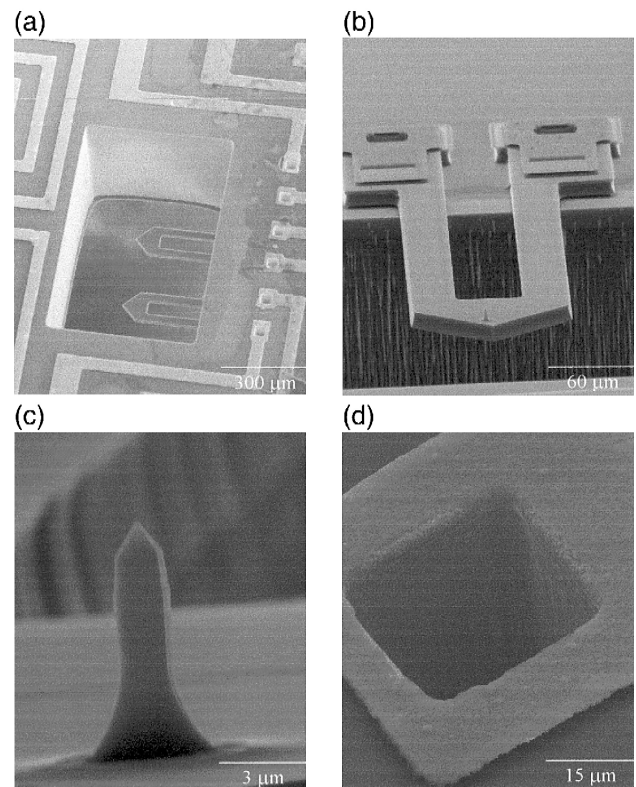


Fig. 3. SEM micrographs of completed cantilever arrays. (a) Backside view, looking through to cantilevers on the front. (b) An individual piezoresistive cantilever, (c) silicon tip, and (d) through-wafer interconnect.

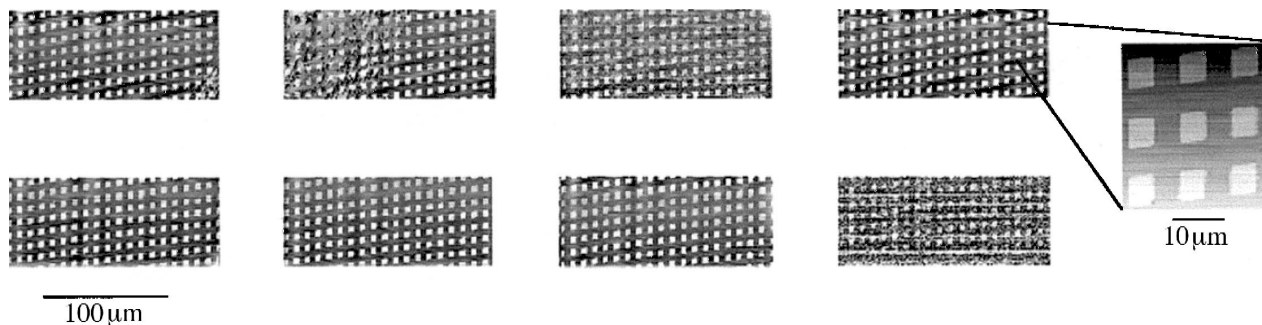


Fig. 4. Parallel image of a grating (10 μm pitch, 0.2 μm step) with a 2×4 array of piezoresistive cantilevers. The cantilever pitch is 250 μm horizontally, and 1500 μm vertically. Each cantilever sweeps out a $170 \times 70 \mu\text{m}^2$ area by scanning at 560 $\mu\text{m}/\text{s}$. The entire image is scanned in 140 s. A scratch on the grating is visible across the top left two cantilevers.

as a membrane over the 30 μm squares. With this resist mask the aluminum is wet etched, and the tungsten, polysilicon, and nitride layers on the tip side and wire bonding side of the wafer are patterned in SF_6 plasma etches. The etch stops on the oxide, preserving the sharp tip, and the oxide is removed in BHF (Fig. 2d).

After completing the TWV, the cantilevers are released with a backside etch (Fig. 2e), again using an HDP etch which stops on the buried oxide [20]. The anisotropy of this technique allows for small release regions and thus high cantilever density. The buried oxide is then removed in BHF. The resist that protects the cantilevers is stripped in oxygen plasma for the final release (Fig. 2f).

3. Results

Completed cantilevers were 10 μm thick, 200–400 μm long, and have 7- μm tall tips (Fig. 3). An off-chip Wheatstone bridge circuit followed by a 10^5 gain stage was used to monitor changes in each cantilever's piezoresistance. Deflection sensitivities of 10^{-7} nm^{-1} to $5 \times 10^{-7} \text{ nm}^{-1}$ and minimum detectable deflections of 10–20 \AA (10 Hz–1 kHz bandwidth) were measured on suspended cantilevers. The designed resistance was 1 k Ω for each piezoresistor plus its interconnect. While this was achieved on test wafers (not SOI), device wafers had overall resistances of 3–13 k Ω . This is attributed to over-etching of the buried oxide during the TWV etch, which lead to poor metal deposition in this region.

To demonstrate functionality, a 2×4 cantilever array was used to image an arbitrary location on a grating (Fig. 4). After the bridge gains and offsets were individually tuned for each cantilever, the cantilever array was aligned to the sample. Tip-height uniformity was adequate to enable manual alignment of the chip to the sample. Each cantilever scanned $170 \times 70 \mu\text{m}^2$, while their signals were simultaneously collected by a computer; the entire scan was acquired in 140 s. The fact that the sample was much larger than the cantilever array (1 cm^2 vs. 0.5 mm^2) demonstrates the utility of TWV integration.

The fabrication process is scalable to larger and denser arrays, and can be integrated with other unique sensor topologies. Chip-scale alignment for passive cantilever arrays is possible, as demonstrated here and elsewhere, but integrated actuators for each cantilever are desirable for enabling parallel non-contact imaging and for aiding in alignment [16–18]. Though specific parameters depend on the application, it is reasonable to consider arrays of thousands of probes scanning centimeter distances in tens of seconds. Increasing throughput through parallelism is particularly attractive for scanning probes, because it allows larger sample regions and shorter acquisition times, while maintaining functional versatility and force sensitivity.

4. Conclusion

Through-wafer interconnects have been integrated with a two-dimensional array of piezoresistive cantilevers. Scanning of an arbitrary location on a sample is demonstrated by imaging with 2×4 array. The successful integration of TWVs with micromachined sensors will have broad applications elsewhere in the MEMS community.

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