AIP Advances

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Citation: AIP Advances **3**, 102119 (2013); doi: 10.1063/1.4826583
View online: http://dx.doi.org/10.1063/1.4826583
View Table of Contents: http://scitation.aip.org/content/aip/journal/adva/3/10?ver=pdfcov
Published by the AIP Publishing

Diode behavior in ultra-thin low temperature ALD grown zinc-oxide on silicon

Nazek El-Atab,[1] Samar Alqatari,[1] Feyza B. Oruc,[2,3] Tewfic Souier,[1] Matteo Chiesa,[1] Ali K. Okyay,[2,3] and Ammar Nayfeh[1]
[1]*Institute Center for Microsystems – Imicro, Department of Electrical Engineering and Computer Science (EECS), Masdar Institute of Science and Technology Abu Dhabi, United Arab Emirates*
[2]*Department of Electrical and Electronics Engineering, Bilkent University, 06800 Ankara, Turkey*
[3]*UNAM-National Nanotechnology Research Center and Institute of Materials Science and Nanotechnology, Bilkent University, 06800 Ankara, Turkey*

(Received 5 September 2013; accepted 10 October 2013; published online 18 October 2013)

A thin-film ZnO(n)/Si(p+) heterojunction diode is demonstrated. The thin film ZnO layer is deposited by Atomic Layer Deposition (ALD) at different temperatures on a p-type silicon substrate. Atomic force microscopy (AFM) AC-in-Air method in addition to conductive AFM (CAFM) were used for the characterization of ZnO layer and to measure the current-voltage characteristics. Forward and reverse bias n-p diode behavior with good rectification properties is achieved. The diode with ZnO grown at 80°C exhibited the highest on/off ratio with a turn-on voltage (V_{ON}) ~3.5 V. The measured breakdown voltage (V_{BR}) and electric field (E_{BR}) for this diode are 5.4 V and 3.86 MV/cm, respectively. [http://dx.doi.org/10.1063/1.4826583]

Extensive research is being conducted on the II-VI compound semiconductor zinc oxide owing to its optoelectronics properties and its wide technological applications. ZnO has been extensively studied recently in thin film transistors (TFTs), light emitting diodes (LED), and solar cells.[1–3] For low-cost flexible electronics, low temperature techniques are of critical importance. Sputtering, Atomic Layer Deposition (ALD), solution-based techniques, and pulsed laser deposition are some of the methods used to deposit ZnO.[3–14] ALD technique has grown in importance over the last years because it can achieve large area uniformity, precise thickness control, highly conformal deposition, and most importantly; it can be applied under low temperature growth which is crucial for the fabrication of low cost and flexible electronics. Earlier we showed a working SONOS memory using ALD grown ZnO.[15] In this work a ZnO/Si heterojunction n-p diode is grown by ALD and demonstrated by Conductive Atomic Force Microscopy (CAFM).

Before device fabrication processes, silicon wafers are placed in piranha solution (H_2SO_4:H_2O_2 (4:1) ratio) for ten minutes in order to remove organic residues from the surface. Then the wafers are placed in dilute HF acid solution to remove native oxide and achieve hydrophobic surfaces for efficient device fabrication. The heterojunction diode is then fabricated by depositing 14 nm of ZnO by ALD at different temperatures on highly doped (5×10^{18}/cm^3 Boron) p-type (100) Si wafer. ALD-deposited ZnO is n-type due to native crystallographic defects such as interstitial zinc and oxygen vacancies which behave as electron donors.[15] The polycrystalline nature of the deposited ZnO is analyzed by X-Ray Diffraction (XRD) measurements. All of the ALD grown ZnO thin films exhibit "*hexagonal wurtzite*" structure with characteristic XRD peaks at (100), (002), (101), (102), (110), (103) and (112) crystal orentations as shown in Fig. 1, indicating the formation of good polycrystalline ZnO thin films through ALD method.

After the ALD growth, AFM AC-in-Air method in addition to CAFM were used for the characterization of ZnO layer deposited at 80° and 130° on Si wafer. The AFM used is an Asylum

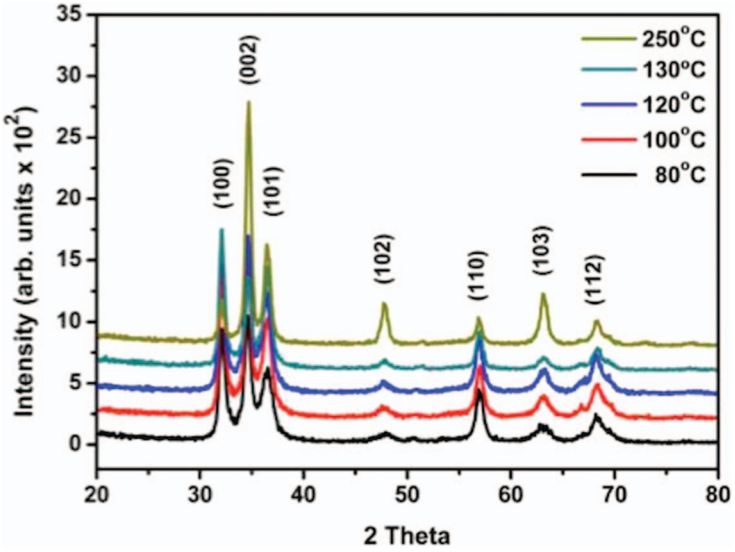

FIG. 1. XRD data of ZnO thin films grown at various temperatures.

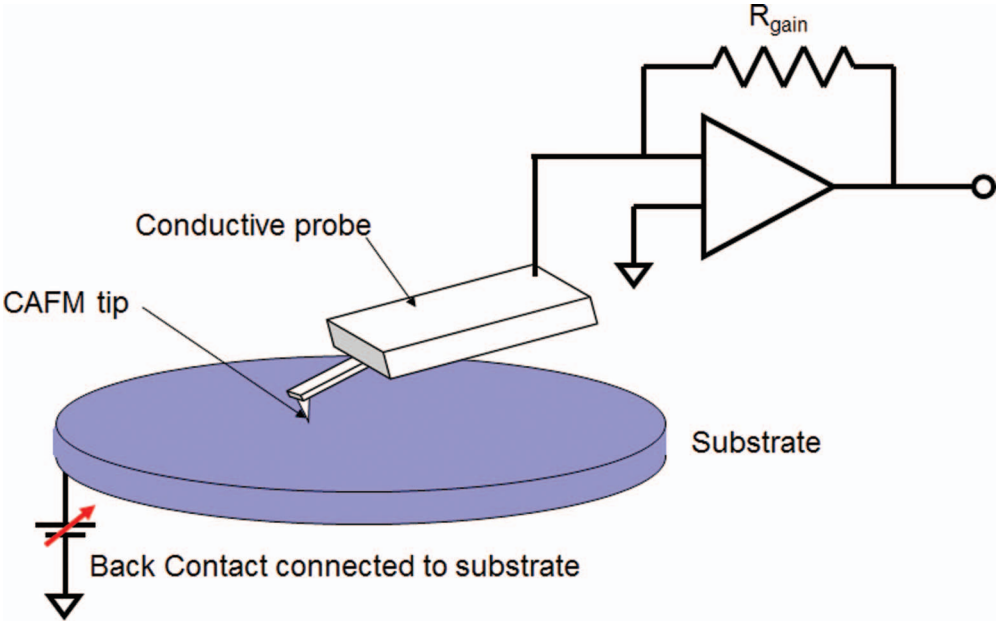

FIG. 2. CAFM setup showing the conductive probe and the transimpedance amplifier used to detect the current flow.

Research MFP-3D, with a dual-gain CAFM module for the electrical measurements. For topography imaging AC-in-Air method was used. The electrical mapping was done in contact mode using the dual-gain module.

The CAFM setup is shown in Fig. 2. As a matter of fact, testing the conductivity of the samples using the AFM is made possible in two ways: probing them horizontally allows for analyzing the electric properties of the ZnO thin film solely, while probing them vertically allows for analyzing the electric properties of the ZnO-Si junction, locally, as a whole. In this paper, we use the vertical approach of using conductive AFM to measure the local properties of the ZnO-Si junction, and apply voltage on the sample vertically. In order to perform conductive AFM, the electrode was in contact with a metal base, which the samples were put in contact with using silver paste. A diamond probe was used to test for conductivity under contact mode, while a silicon probe was used for collecting

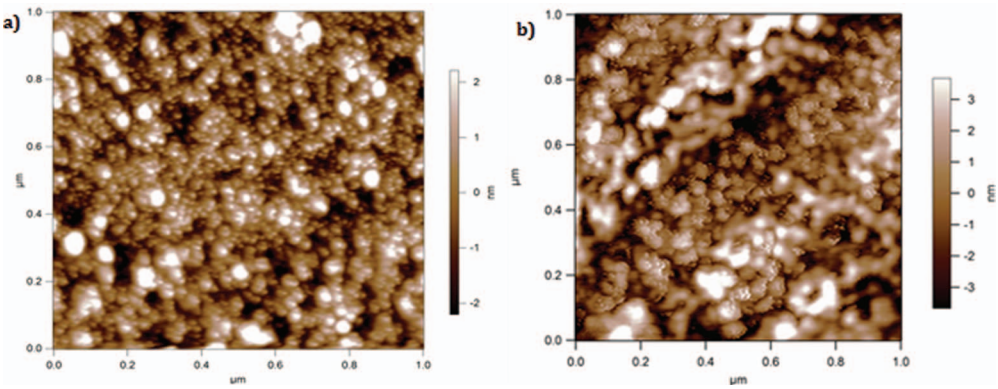

FIG. 3. Topography image of ZnO layer deposited by ALD a) at 80° b) at 130°.

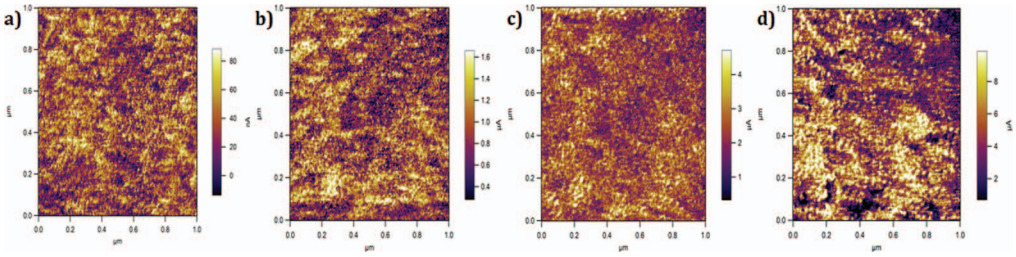

FIG. 4. Surface conductivity of 80° sample with different applied surface voltages. a) 1V, b) 2V, c) 3V, d) 4V.

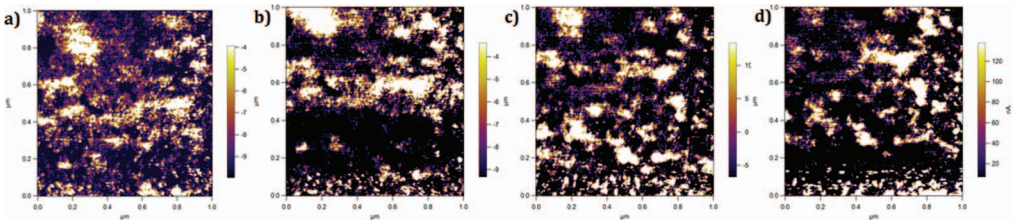

FIG. 5. Surface conductivity of 130° sample with different applied surface voltages. a) 1V, b) 2V, c) 3V, d) 4V.

topography images in AC mode. In the conductivity experiments, the current flows between the tip and the sample, generating surface conductivity images and I-V curves at selected points, for the ZnO-Silicon sample.

1×1 um^2 topography images were obtained of both 80° and 130° samples as shown in Fig 3(a) and Fig. 3(b), respectively. The surface roughness of the two samples did not significantly differ: the extracted surface RMS roughness is around 1.7 nm for the 80° sample, and 1.1 nm for the 130°. For the 80° sample; the biggest particle size was 60 nm and the smallest particle was 20 nm, while for the 130° sample; the biggest particle size was 60 nm and the smallest particle was 15 nm. This confirms that the deposited layer of ZnO is more of a continuous film rather than discrete islands. Furthermore, surface conductivity images were obtained for different applied surface voltages and at different locations. The surface conductivity images of the 80° and 130° samples depicted in Fig. 4 and Fig. 5, respectively, show that the the 80° sample surface conductivity is higher than the 130° sample. However, more measurements are still needed to confirm this finding. In addition, Fig. 4 and Fig. 5 portray non-homogeneous electric behavior across the surface of the thin film, despite its smoothness. The more conductive parts, as shown in the images, do not correlate to the grains or features shown in the topography images shown in Fig. 3. The inhomogeneity of the surface

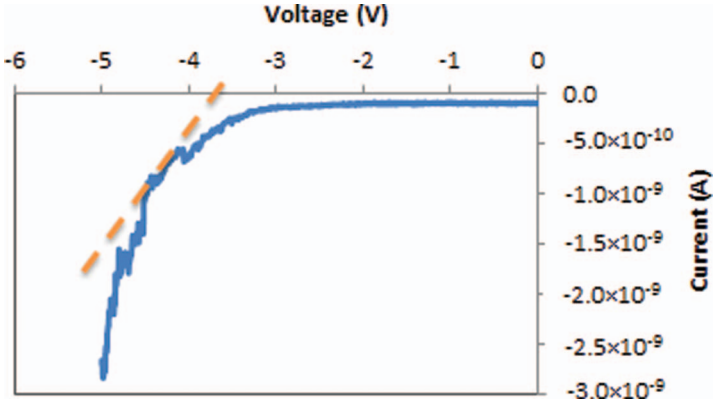

FIG. 6. Measured forward bias of the 80° diode showing a V_{ON} of 3.5 V.

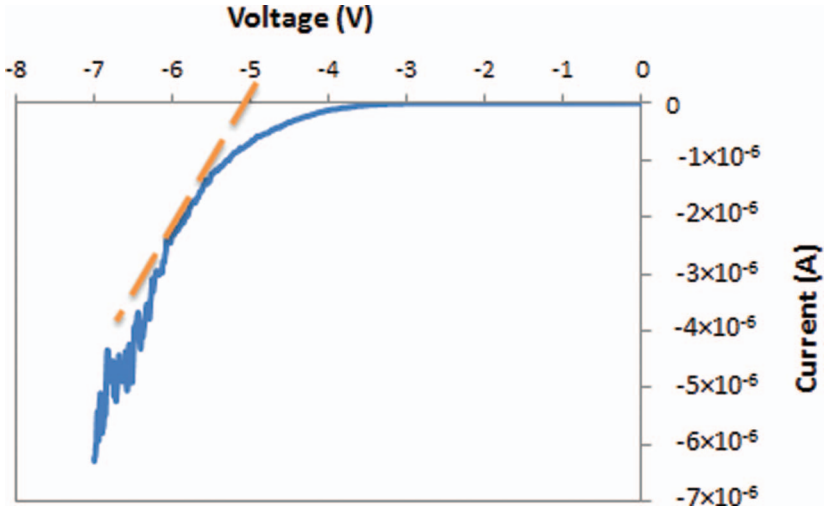

FIG. 7. Measured forward bias of the 130° diode showing a V_{ON} of 5 V.

conductance could be attributed to grains of Si, defects in the thin film deposition, or the growth temperature, but the reason behind the inhomogeneous conductive behavior could not be verified.

Additionally, CAFM detects the resulting current flow using a transimpedance amplifier.[16] Using this technique, I–V characteristics of the ZnO(n)/Si(p) device can be obtained. Fig. 6 and Fig. 7 plot the transfer characteristic (I-V) of the 80° and 130° samples, respectively, in the forward bias with the voltage being swept from 0V to −6V. The results exhibit a diode-like forward bias curve with a turn-on voltage of ∼3.5 V for the 80° sample while 5 V for the 130° sample. Also, the transfer characteristic (I–V) of the 80° sample in the reverse bias is shown in Fig. 8 with the voltage being swept from 0 to 6 V. In this sweep, an exponential increase in current is not seen due to the large barrier in reverse bias, as expected. Rather, a sharp increase in current is observed at around 5.4V which is more consistent with diode breakdown. This breakdown could be due to tunneling (zener) or impact ionization (avalanche). Using this breakdown voltage ($V_{BR} = 5.4V$), the breakdown electric field (E_{BR}) of the 14 nm ZnO layer is extracted to be 3.86 MV/cm. However, the 130° sample didn't show any reverse bias curve when the voltage was being swept from 0 V up to 6 V. Furthermore, the ZnO/Si heterojunction diode that has been fabricated based on 80°C-ALD-grown ZnO thin film exhibited the highest electrical rectification characteristics with an ON/OFF ratio reaching up to 10^3 as shown in Fig. 9.

The existence of a critical breakdown field in reverse bias and exponential increase in forward bias with the 80° sample confirms the creation of n-p heterojunction diode. Table I summarizes

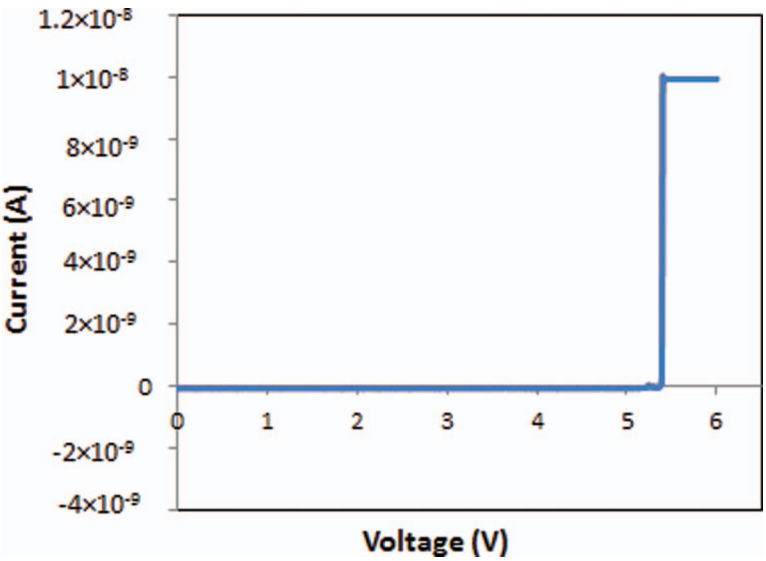

FIG. 8. Measured reverse bias of the n-p ZnO/Si diode with V_{BR} of 5.4 V.

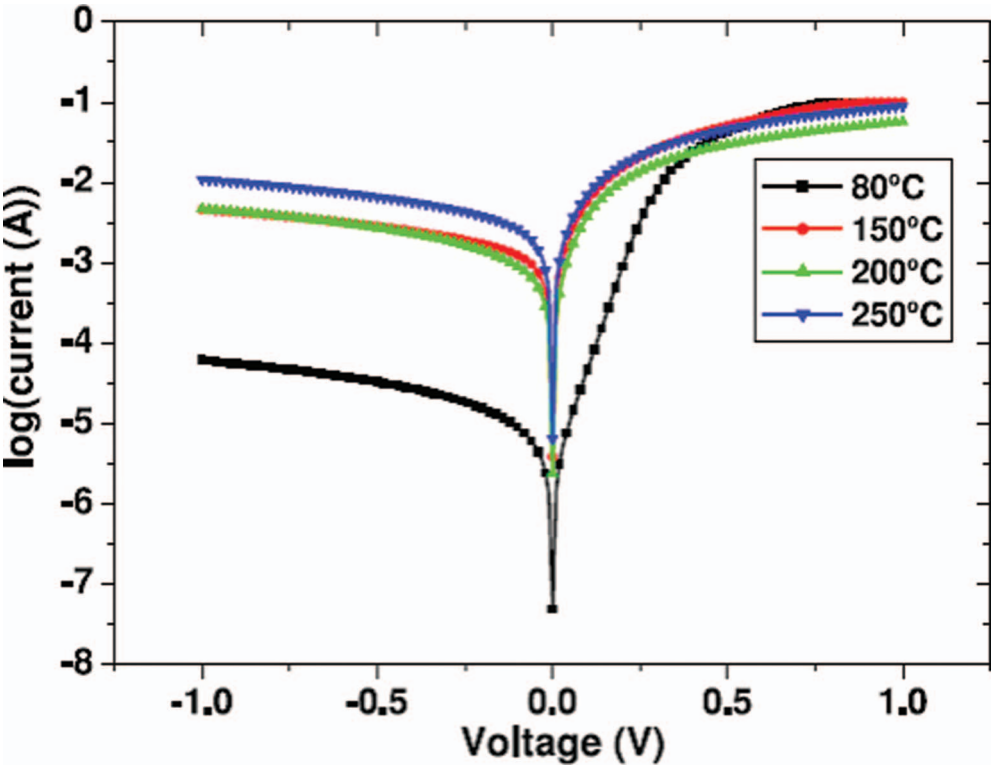

FIG. 9. Dark current (I) versus bias voltage (V) spectrum of the fabricated ZnO-Si diodes.

the results obtained for the diode with ZnO grown at 80° with key parameters $V_{BR,}$ E_{BR}, and $V_{ON.}$ Moreover, the equilibrium energy band diagram of the ZnO(n)/Si(p) diode is represented in Fig. 10. The conduction and valence band offsets (ΔE_c and ΔE_v) between Si and ZnO are 0.4 eV and 2.55 eV, respectively.[17] From the energy band diagram, it is shown that there is a 0.4 eV barrier for electrons and 2.55 eV barrier for holes. In the reverse bias, the barriers increase and hence the

TABLE I. Extracted values of V_{BR}, E_{BR}, and V_{ON} of the n-p diode with ZnO grown at 80°C.

V_{ON}	3.5 V
V_{BR}	5.4 V
E_{BR}	3.86 MV/cm

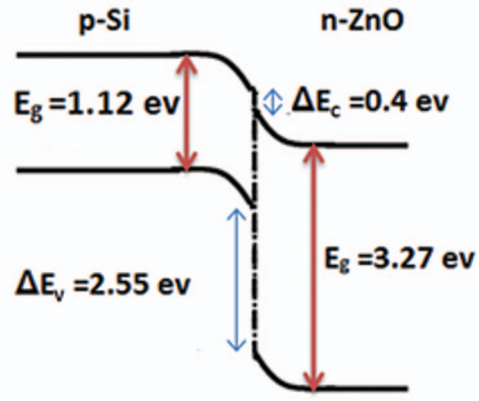

FIG. 10. Energy band diagram of the heterojunction n-ZnO/p-Si at zero voltage bias. The diagram shows the barrier for the electrons and holes.

low current is observed. At high enough electric field, tunneling or impact ionization dominates leading to breakdown.

In summary, a heterojunction diode was fabricated by low temperature ALD deposition of 14 nm of ZnO on silicon (p+) substrate. The current voltage characteristic measured is consistent with an n-p diode. The results showed that the diode with ZnO grown at 80° exhibited higher on/off ratio, and lower turn on voltage and turn on current than the 130° grwon ZnO. Moreover, the results highlight the possible use of this ZnO low cost, flexible, and transparent electronic applications and for future low cost thin film photovoltaic cells.

ACKNOWLEDGMENTS

We gratefully acknowledge Dr. Sabri Alkis and Amro Alkhatib for their contributions in the experiments and analysis provided in this paper.

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