

Graphene field effect devices operating in differential circuit configuration



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ABSTRACT

We study the concept of a basic building block for circuits using differential signaling and being based on graphene field effect devices. We fabricated a number of top-gated graphene FETs using commercially available graphene and employing electron beam lithography along with other semiconductor manufacturing processes. These devices were then systematically measured in an automated setup and their DC characteristics analyzed in terms of a simple but effective analytical model. This model together with the collected data allowed us to proceed further with both mathematical analysis of circuit characteristics as well as numerical simulation in a dedicated circuit analysis software.

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1. Introduction

After decades of miniaturization and performance tuning, silicon electronics is approaching its technological limits [1]. In the search for alternative transistor channel materials, graphene has been given much attention since its discovery in 2004 [2], mainly because it offers compelling values of carrier mobility and a consequent potential for high frequency operation, possibly reaching into the THz range [3]. Certain drawbacks however, such as the weak or absent current saturation or the high “off” current, limit the use of graphene for traditional CMOS-like circuitry [4]. Elementary circuits based on graphene devices, such as an audio voltage amplifier [5] or a logic inverter [6] have already been published. They rely, however, on CMOS-like principles to operate, whereas in this work we investigate the possibility of employing graphene devices for an alternative approach based on differential signaling, where saturation and off-current are not expected to preponderate.

2. Device fabrication

We used samples of commercially available, CVD-grown single layer graphene, transferred onto a silicon substrate covered by 285 nm of SiO₂ (Fig. 1). Channel regions were defined by removing graphene in the surrounding areas by an ion-beam etch. Cr/Au

source and drain (S/D) contacts were evaporated and patterned by electron beam lithography (EBL) and lift-off, followed by atomic layer deposition (ALD) of a 15 nm thick Al₂O₃ gate dielectric. Finally, the gate electrode is patterned and deposited similarly to the S/D electrodes. The gate dielectric, which also covers the S/D metal prevents a short circuit with the gate electrode and allows for tight alignment, reducing the length of un-gated channel regions to a minimum. An example of fabricated graphene FET (GFET) is shown in Fig. 2.

3. Characterization and data analysis

Electrical measurements were taken to assess the transistor's DC characteristic. An automated setup was used to apply identical measurement conditions to a large quantity of devices. The resulting drain current vs gate voltage $I_D(V_G)$ and drain current vs drain voltage $I_D(V_D)$ curves were analyzed in terms of several key parameters, using the following expressions for fitting:

$$G_{ds} = \sqrt{g_m'^2 (V_G - V_0) + g_0^2}, \quad (1)$$

where G_{ds} is the transistor's overall conductance between source and drain, g_m' is the transconductance per unit of drain-source bias ($g_m' = g_m/V_{ds}$), V_0 is the Dirac voltage, and g_0 is the conductance minimum at the Dirac point ($G_{ds}(V_G = V_0) = g_0$). For simplicity g_m' and g_0 will be referred to as reduced transconductance and base conductance respectively throughout this paper.

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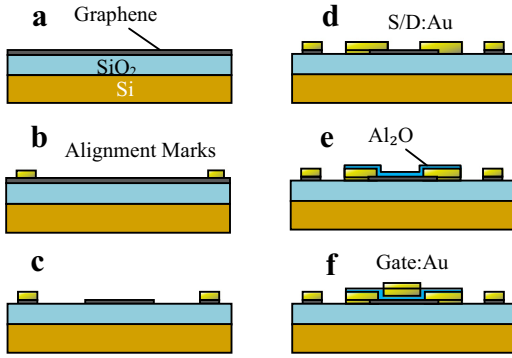


Fig. 1. Fabrication process flow. (a) Substrate Si, 512 μm + SiO_2 , 285 nm + graphene (b) alignment marks, Cr/Au (c) graphene etch (d) S/D contacts, Cr/Au (e) gate dielectric, Al_2O_3 ; (f) gate metal.

This intrinsic conductance translates into an extrinsic output current, when taking the contact resistances into account ($R_S = 2R_C$):

$$I_{\text{extr}} = V_{DS} \frac{G_{ds}}{1 + R_S G_{ds}}. \quad (2)$$

These are responsible for the concave bending and eventual saturation of the $I_D(V_D)$ curve far away from the Dirac point. No other current saturation effects, such as carrier velocity saturation due to scattering mechanisms (MOSFET-like pinch off does not exist in gapless single layer Graphene [7]), are taken into account here.

This simple model, albeit empirical rather than based on physics principles, provides excellent fitting results and allows extracting parameters that reflect the device's extrinsic performance relevant for circuit simulation. Similar models, also containing square-root based expressions but tailored to extract physical rather than circuit-relevant parameters were used in the past, e.g. by Meric [8,9] and Scott [10]. It may also be more suitable for hand calculations in the analysis of elementary circuits than complex physical models. Combining a series of $I_D(V_G)$ curves, measured at different drain bias values, and performing a surface fit allows capturing the complete DC characteristic of a device. Surface fits obtained in this manner exhibit a slightly larger residual error compared to individual curve fit but are still acceptable for our purpose (Fig. 3).

4. Differential circuit modeling

The working principle of the differential pair circuit relies on a constant current source in the stem and two switching devices

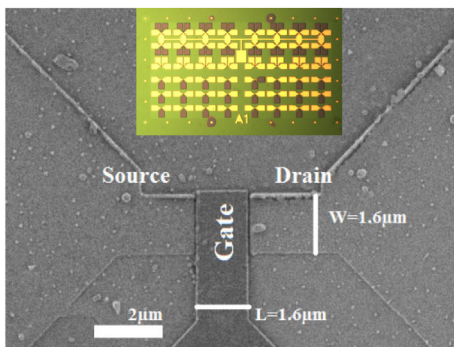


Fig. 2. SEM image of a single graphene FET, with $L = 1.6 \mu\text{m}$ and $W = 1.6 \mu\text{m}$ (to protect the graphene from electron irradiation device was imaged after electrical characterization – hence the contamination). Inset: microscope image of an array of devices, one of 12 per die.

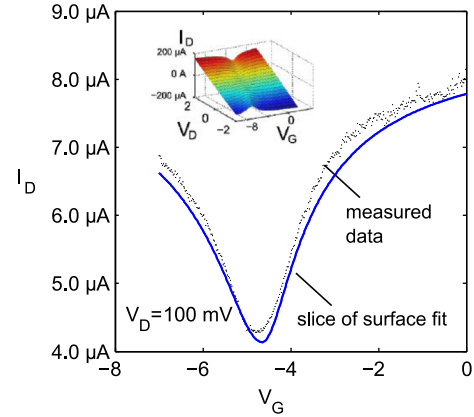


Fig. 3. Typical $I_D(V_D)$ curve. The fit is obtained from multiple $I_D(V_G)$ measurements on the same device with varying V_D . Inset: extrapolation of complete current-voltage characteristic.

directing the current in either one or the other of two “branches” (Fig. 4). The sum of the currents of both branches is therefore constant. The switching effect can be described by an imbalance factor α :

$$\alpha = \frac{I_1 - I_2}{I_S} \quad (3)$$

where $I_S = I_1 + I_2$ is the stem current supplied by the constant current source. In this formulation, the branch currents become

$$I_{1,2} = \frac{1}{2}(1 \pm \alpha) \cdot I_S \quad (4)$$

The output voltage is the difference of the drain nodes in either branch of the circuit:

$$V_{D1,2} = V_{DD} - R_L I_{1,2} \quad (5)$$

$$V_{\text{out}} = V_{D1} - V_{D2} = R_L(I_2 - I_1) = -\alpha R_L I_S \quad (6)$$

If we model the graphene devices as conductances G_1 and G_2 (which are each a function of the devices' bias conditions, i.e. V_G) then the total resistance of each branch can be expressed as

$$R_{br,i} = R_L + 1/G_i. \quad (7)$$

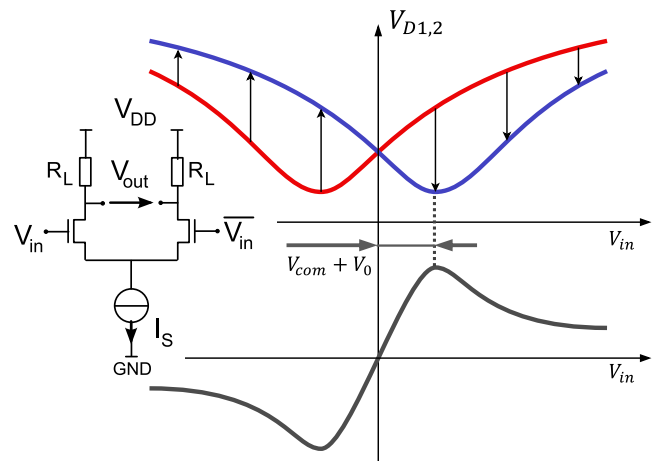


Fig. 4. Circuit schematic (inset) and simplified working principle of the graphene differential pair. Upper axis: left (red) and right (blue) transistor output (drain) voltage, V_D . Lower axis: transfer curve, V_{out} , determined by subtraction of blue curve from red curve. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

Since the voltage drop on both branches is necessarily identical, we can write $R_{br1}I_1 = R_{br2}I_2$. Combining this with Eqs. (4) and (7) yields

$$\frac{R_L + 1/G_2}{R_L + 1/G_1} = \frac{1 + \alpha}{1 - \alpha} \quad (8)$$

which can be rearranged and solved to find the imbalance factor, as follows

$$\alpha = \frac{G_1 - G_2}{G_1 + 2G_1G_2R_L + G_2}. \quad (9)$$

This result is independent of the bias conditions V_{DD} and I_S and reflects the circuit's intrinsic performance. For G_1 and G_2 we can substitute a modified version of Eq. (1) in which we replace $V_G = V_{com} \pm V_{in}$ respectively, where V_{com} is the common offset voltage around which the input voltage V_{in} is varied. Note that, as a simplification, the (common) source voltage, V_S , is not taken into account. Whereas the relevant parameter for the channel conductance modulation is $V_{GS} = V_G - V_S$ rather than simply V_G we assume here a source voltage of 0 V in order to maintain the analytic expressions at a manageable complexity. In practice, for numerical computations, we select a value of V_{com} to which we add the term $V_{DD} - I_S(R_L + 1/g_0)$ thus compensating for a nonzero, constant V_S . The circuit's transfer function is thus

$$V_{out} = H(V_{in}) = -\alpha(V_{in})R_LI_S. \quad (10)$$

The transfer curve is schematically illustrated in Fig. 4. Its appearance is dominated by the subtraction of the output characteristic of one device with the other's, resulting in a useful, linear region between a negative and a positive peak value. These peaks correspond to the Dirac point of each device respectively, their position on the input voltage's axis is related to $V_{com} + V_0$ as illustrated in the figure. The principal figures of merit of this differential pair are the input swing, characterized by the relative distance between the Dirac peaks in the transfer curve, as well as the slope and linearity of the linear region in-between. The slope can be computed by taking the derivative

$$S'(V_{in}) = \frac{\partial}{\partial V_{in}} R_L \alpha(V_{in}). \quad (11)$$

Note that S' is the slope per unit of bias current, I_S , bearing the unit 1/A; we define the actual slope as $S = I_S \cdot S'$. The result is rather unwieldy but can be evaluated at $V_{in} = 0$, resulting in

$$S'(0) = \frac{g_m^2 R_L}{G_0^2 + R_L G_0^3} (V_0 - V_{com}), \quad (12)$$

where $G_0 = \sqrt{g_m^2 (V_0 - V_{com})^2 + g_0^2}$.

Parameters that can be independently tuned to optimize the circuits' performance include the common mode of the input signal V_{com} and the pull up resistances R_L . Fig. 5 displays the slope versus each of these parameters. In order to maximize the slope, there is an optimum value for V_{com} beyond which not only the slope but also the linearity decrease. This optimum value can be very close to the symmetry point ($V_{in} = 0$) and approaches it further as transconductance improves. In terms of the load resistance, the slope monotonically increases with the value of R_L , but the benefit of increasing R_L further diminishes gradually as the slope approaches its asymptotic value.

Theoretically, both R_L and I_S could be multiplied at will in order to boost the circuit's amplification. However, the value of V_{DD} required to keep the current source from saturating may quickly reach prohibitive levels. Instead it will be advisable to carefully tune the balance between R_L and I_S such as to obtain an effective drive current while limiting the voltage drop across the load resistors.

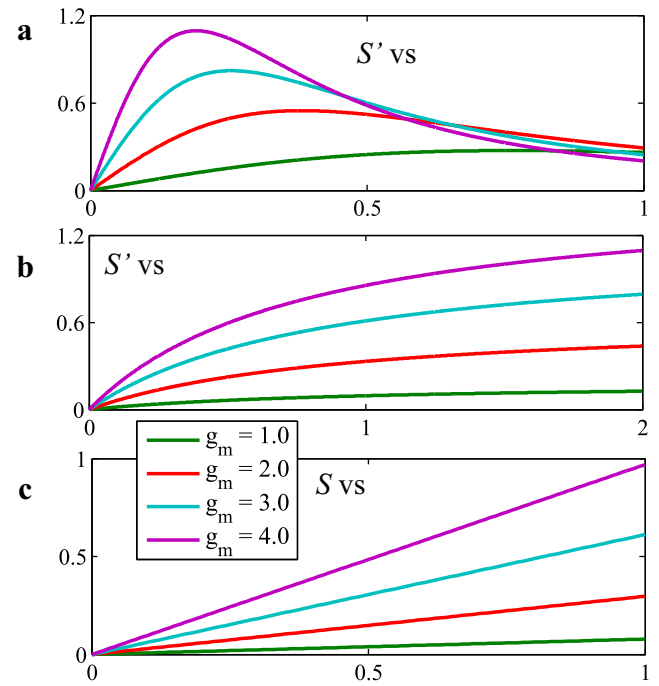


Fig. 5. Slope S' of the transfer curve at $V_{in} = 0$ for different values of g_m , as a function of (a) V_{com} and (b) R_L and (c) S as a function of I_S . Variables are normalized according to Table 1.

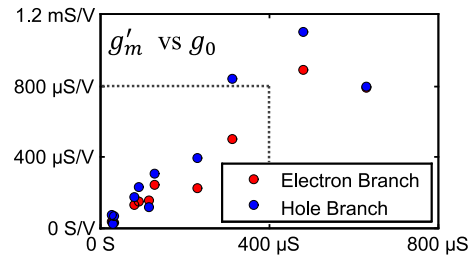


Fig. 6. Scatter plot of the reduced transconductance g'_m vs the base conductance g_0 of a multitude of devices with varying dimensions.

Table 1

Typical values and normalization of main parameters. All parameters of a particular unit share the same normalization factor.

Parameter	Unit	Typical value	Normalization factor	Normalized value
g'_m	S/V	800 μ S/V	400 μ S/V	2
g_0	S	400 μ S	400 μ A	1
V	V	1 V	1 V	1
I_S	A	400 μ A	400 μ A	1
R_L	Ω	2.5 k Ω	1/400 μ S	1
S'	1/A	2.5 μ A $^{-1}$	1/400 μ A	1

For realistic numerical modeling, it is crucial to assess the relationship between the model's two main parameters, g'_m and g_0 . Measurement data presented in Fig. 6 reveals a linear trend where $g'_m \approx \chi g_0$, with the proportionality constant $\chi = 2$. This trend is interesting since it is desirable to have both a high value of g'_m and a low value of base conductance, g_0 . It appears, however, that it is not possible to improve one of the parameters independently of the other. The values in Table 1 are chosen accordingly.

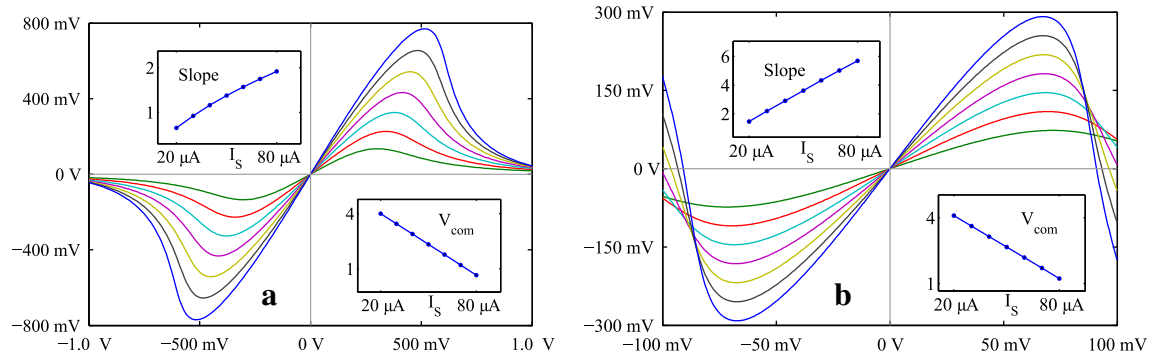


Fig. 7. Differential input–output voltage transfer curves obtained from Verilog-A/Cadence Spectre simulations for different values of I_S , ranging from 20 μA to 80 μA in steps of 20 μA ; the insets on the top left show the slope (voltage gain) at $V_{in} = 0$ for each value of I_S . The insets on the bottom right show the value of V_{com} which were used for the respective bias current level. The device parameters were (a) $g_m = 100 \mu\text{S/V}$, $g_o = 50 \mu\text{S}$, (b) $g_m = 400 \mu\text{S/V}$, $g_o = 40 \mu\text{S}$. In both cases $V_{DD} = 5 \text{ V}$, $V_0 = 0$, $R_L = 3 \cdot (1/g_o)$ and the contact resistance at source and drain were $R_C = 1 \text{ k}\Omega$.

5. Circuit simulation

With the same model and the coefficients obtained from a surface fit of a series of $I_D(V_G)$ as well as $I_D(V_D)$ curves, we programmed a compact model in Verilog-AMS for use with a circuit simulator, in this case CADENCE/Spectre. This approach allows for more flexibility as well as complexity in the circuit design compared to the analytical derivations. In particular it allows taking the contact resistances into account that tend to be on the order of the base conductance.

The results depicted in Fig. 7a shows a fairly linear transfer curve in the input voltage range roughly between -1 V and $+1 \text{ V}$, depending on the bias current. The tradeoff is between input swing and voltage gain (steepness of the transfer curve), which reaches a slightly amplifying value of 1.4. Here we adjusted I_S and R_L for a supply voltage level of 5 V.

In order to achieve higher values of the amplification factor, we analyzed characteristics of graphene FETs previously reported. We found that devices with very low values of g_o can significantly boost our differential circuit's performance (Fig. 7b). We extracted the characteristics from $I(V)$ curves of bilayer graphene devices presented in reference [11], where the values of g_m and g_o were found to be on the order of 400 $\mu\text{S/V}$ and 40 μS respectively (at $V_{bg} = -80 \text{ V}$). The low base conductance is due the band gap opening in bilayer graphene when applying an electric field via a back gate bias V_{bg} . However, as mentioned above, the price to pay for the higher voltage gain is a drastically reduced input swing.

6. Conclusions

We obtained a useful circuit model based on measured current–voltage characteristics of actual graphene devices. This

allowed us to estimate the behavior of a circuit comprised of two GFETs and other circuit elements. Such circuit elements could be used as building blocks in future RF and differential logic electronics applications.

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