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Memory effect by charging of ultra-small 2-nm laser-synthesized solution processable Si-nanoparticles embedded in Si–Al_2O_3–SiO_2 structure

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A memory structure containing ultra-small 2-nm laser-synthesized silicon nanoparticles is demonstrated. The Si-nanoparticles are embedded between an atomic layer deposited high-κ dielectric Al_2O_3 layer and a sputtered SiO_2 layer. A memory effect due to charging of the Si nanoparticles is observed using high frequency *C–V* measurements. The shift of the threshold voltage obtained from the hysteresis measurements is around 3.3 V at 10/−10 V gate voltage sweeping. The analysis of the energy band diagram of the memory structure and the negative shift of the programmed *C–V* curve indicate that holes are tunneling from p-type Si via Fowler–Nordheim tunneling and are being trapped in the Si nanoparticles. In addition, the structures show good endurance characteristic ($>10^5$ program/erase cycles) and long retention time (>10 years), which make them promising for applications in non-volatile memory devices.

1 Introduction Novel ways to increase the stored charge density and reduce the operating voltage of charge trapping memory structures are of vital interest [1–3]. Recently, memories with embedded nanoparticles in the dielectrics have received considerable attention because of their high endurance, low operating voltage, large retention time, and reduced power consumption [4–6].

Many materials such as Si, Ge, SiGe, Au, silicide and Pt have been considered as promising candidates for the charge storage nodes in charge trapping memories. Although several groups of researchers have demonstrated that Si nanoparticles (Si-NPs) have very promising properties for storage of electrical charge for future memory devices, however, most of the published works study >5-nm Si-NPs [5–8]. Technologically feasible and competitive future devices require nanoparticles of sub 3-nm dimensions; a zero-dimensional regime where important modifications to the silicon electronic structure occur. As a matter of fact, the properties of the nanoparticles are strongly dependent on their size; specifically, nanoparticles with diameter below 3-nm have a larger band gap due to quantum confinement in 0-D, smaller dielectric constant [9], larger work-function, smaller electron affinity, and larger charging energy than larger nanoparticles [10].

Various techniques have been generated to synthesize Si-NPs including laser ablated Si target [11], Si ion implantation [12], and the thermal annealing of Si grown by electron-beam evaporation [12, 13] or co-sputtering [14] with the dielectric mixture layers.

In our previous works, MOSFET-based memory cells with 2-nm laser synthesized Si-NPs have been demonstrated and have shown great performance [4, 7]. In this work, a simpler and lower-cost memory device is fabricated using the MOSCAP structure. The memory stack consists of the following layers: metal/high-κ dielectric Al_2O_3/2-nm laser synthesized Si-NPs/SiO_2/p-type. The effect of embedding 2-nm Si-NPs in such memory structure is studied using *C–V* characteristics.

2 Experimental The ultra-small 2-nm average size Si-NPs are fabricated through laser ablation and an acid-free sonication and filtration post-treatment method as reported by Alkis et al. [11]. Figure 1 shows a TEM of the produced non-agglomerate 2-nm average size Si-NPs.

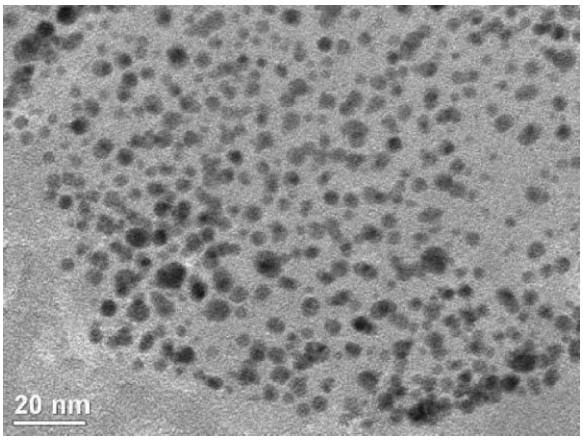

Figure 1 TEM image of the laser-synthesized 2-nm average size Si-NPs.

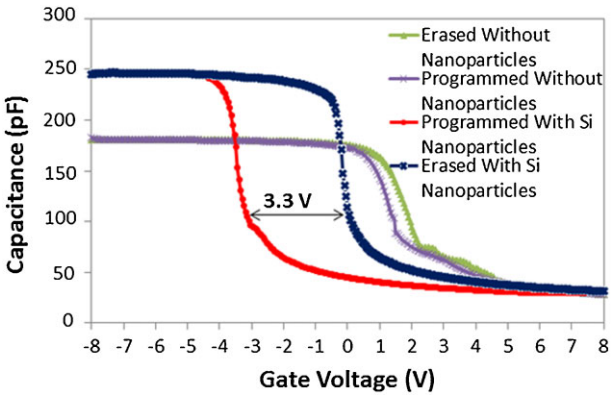

Figure 3 Measured hysteresis behaviour of the C–V_{gate} characteristics with gate voltage sweep at room temperature with and without Si nanoparticles.

The memory cells are fabricated on a p-type (100) (10–20 mΩ cm) Si wafer. Using a Cambridge Nanotech Savannah 100 ALD system, a 5-nm-thick Al_2O_3 oxide is first deposited at 250 °C. Next, Si-NPs are delivered across the sample by spin coating the NPs solution at a speed of 700 rpm and an acceleration of 250 rpm/s for 10 s. Using a shadow mask, a 10-nm-thick SiO_2 blocking oxide followed by a 450-nm-thick Ag layer is sputter deposited. The use of the shadow mask allowed for patterning the metal gate to a circular shape of diameter 1 mm without the need for any lithography or etching steps which greatly reduces the time and cost needed to fabricate such memory cells. It should be mentioned that even though the fabricated memory devices have 1-mm radius, the structure of such MOS memory device is expected to be scalable without degradation of performance according to the ITRS roadmap [15]. A reference memory device without Si-NPs is also fabricated. Figure 2 shows a cross-section of the final device structure with Si-NPs.

3 Results and discussion The charging effect of the Si NPs is analyzed by studying the C–V_{gate} characteristics of the programmed and erased states of memory devices at high frequency (1 MHz). Using the Agilent-Signatone B1505A semiconductor device parameter analyzer, the memory cells gate voltage was first swept from 0 V back to −2 V then forward to 0 V. At this low value of applied gate voltage, there was no observed memory hysteresis and the measured C–V curve was the same as the erased state curve shown in Fig. 3. Then, upon sweeping the gate voltage from −8 to +8 V with a hold time of 20 s at −8 V, there was a near parallel shift in the measured C–V characteristic in the negative direction [negative threshold voltage shift (ΔV_t)] from the uncharged state as seen in Fig. 3. The value of the shift in the V_t is 3.3 V. The V_t is extracted at a capacitance of 100 pF at the onset of the inversion region as shown in Fig. 3. It is worth mentioning that the spin coating technique used in this work does not result in a uniform NPs distribution across the sample as demonstrated in our earlier work [4]. Various methods are being explored for getting uniform NPs distribution [16]. In addition, similar measurements are conducted on a reference memory without NPs and the measured C–V characteristic of the programmed and erased states are shown in Fig. 3 where a negligible V_t shift is achieved. Also, the erased state of the memory without NPs is shifted to the right with respect to the erased state of the memory with NPs, which suggests that the Si-NPs are initially positively charged, however, more research is needed to confirm this finding.

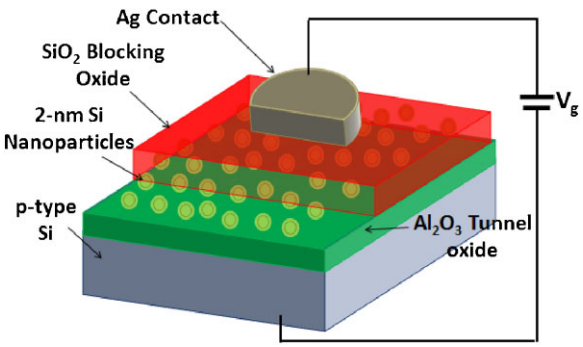

Figure 2 Schematic illustration of the fabricated memory with Si-NPs.

The negative shift in the C–V is due to holes storage in the Si-NPs as described by Eq. (1) [17]

$$V_{FB} = \phi_m - \phi_S - \frac{t_{cntrl} \times Q_s}{\varepsilon_{ox}}, \quad (1)$$

where V_{FB} is the flat-band voltage, ϕ_m is the metal work-function, ϕ_s the channel work-function, Q_s is the areal density of a sheet charge located at a distance t_{cntrl} from the gate electrode, and ε_{ox} is the oxide permittivity. And the threshold voltage equation is

$$V_t = V_{FB} - 2\phi_p + \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2\varepsilon_{Si} q N_A (2\phi_p)}, \quad (2)$$

where ϕ_p is the potential in the Si substrate, t_{ox} is the thickness of the oxide, N_A is the substrate doping, and ε_{ox}, ε_{Si} are the oxide and Si dielectric constants. Therefore, depending on the sign of the stored charge; the flat-band voltage, thus the threshold voltage, can either shift positively for electron charging or negatively for hole charging.

Upon reversing the bias sweep from +8 to −8 V with a 20 s hold time at +8 V, there was a reduction in the stored positive charge, and hence the V_t voltage was observed to shift back to the "uncharged" state as shown in Fig. 3. As a result, based on these *C–V* hysteresis measurements, the storage of holes upon negative gate voltage biasing was the observed programming operation, and the removal of stored holes upon positive bias conditions was the observed erase operation of these memory devices with 2-nm Si-NPs.

The *C–V* measurements were also carried out at 10 kHz. There was small frequency dispersion in the *C–V* curves where the capacitance decreased from 263 to 250 pF at 10 kHz and 1 MHz, respectively. Also, there was hysteresis dispersion where the measured memory hysteresis at higher sweeping rates is larger ($\Delta V_t = 3.3$ V at 1 MHz while $\Delta V_t = 3$ V at 10 kHz) as shown in Fig. 4. This dispersion is usually due to parasitic effect (including back contact imperfection) [18, 19], oxide-tunneling leakage current (direct tunneling current, F–N tunneling etc.) [20], unwanted interfacial layer [21] and dielectric constant (*k*-value) dependence (dielectric relaxation) [22]. However, for gate oxides thicker than 3 nm, it has been already shown that the tunnelling currents are small [23, 24]. As the demonstrated devices have a tunnel oxide thickness of 5-nm and a blocking oxide of 10-nm, it can be safely assumed that tunnelling is not a significant issue in our devices.

In addition, the existence of an interfacial layer between the high-*k* thin film and silicon substrate causes frequency dispersion. It has been reported that the ALD deposition of Al_2O_3 on Si results in a 1-nm SiO_2 interfacial layer [25, 26]. However, the relative thicker thickness of the Al_2O_3 (5-nm) than the interfacial layer (∼1-nm) significantly prevents frequency dispersion [24]. Therefore, the frequency dispersion in the fabricated memory cells can be assumed to be mainly due to the dielectric relaxation (intrinsic cause) and to parasitic effects (back contact imperfection). Annealing the samples and depositing substrate back contact Al would significantly reduce the observed dispersion [24].

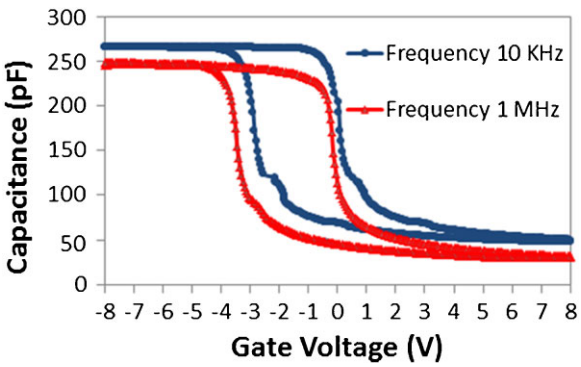

Figure 4 *C–V* characteristics at frequencies of 10 kHz and 1 MHz.

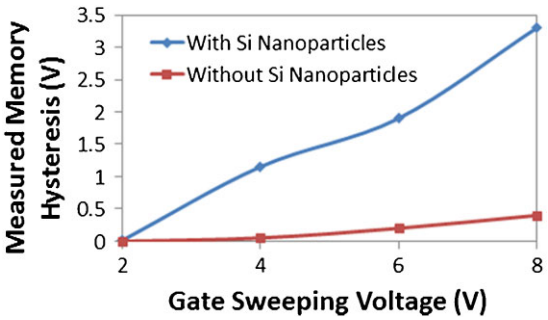

Figure 5 Measured memory hysteresis versus gate sweeping voltage with and without Si-NPs.

Also, the obtained memory hysteresis with and without Si-NPs is measured at different gate sweeping voltages as shown in Fig. 5. Assuming the V_t shift is mainly due to the trapped charges in the Si-NPs, the charge trap states density of the Si-NPs can be calculated by adopting the following equation [27]:

$$Q = \frac{C_t \cdot \Delta V_t}{q}, \tag{3}$$

where C_t is the capacitance of the memory per unit area, ΔV_t is the V_t shift, and q is the elementary charge. For a 3.3 V V_t shift, and C_t (calculated by dividing the high frequency accumulation capacitance by the gate circular area) is 796.18 nF/cm^2; the charge trap states density is roughly 1.9×10^{13} cm^{-2}.

In addition, the energy band diagram of the memory cell with Si-NPs is constructed and shown in Fig. 6. The changes in the electronic structure of the Si-NPs due to quantum confinement in 0-D and to the increased charging energy are taken into account [17]. The Coulomb charging energy of Si-NPs of size 2 nm is calculated to be 1.1 eV using Eq. (4),

$$E = \frac{q^2}{C}, \tag{4}$$

where q is the coulomb charge and C is the capacitance of the NP. Figure 6 shows that there is no conduction band offset

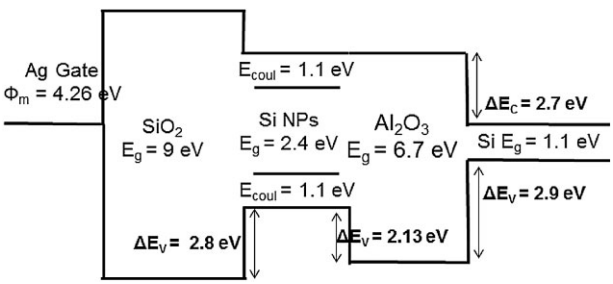

Figure 6 Energy band diagram of the fabricated memory with Si-NPs.

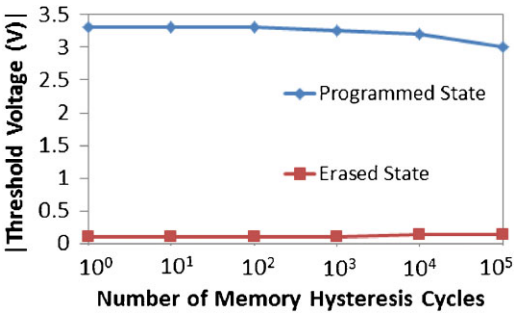

Figure 7 Measured result of the endurance of the memory system showing a high V_t shift after 10^5 program/erase cycles.

between the Si-NPs and the tunnel oxide [17, 28, 29] which might prevent electrons storage; however, the band minimum of the Si-NPs is beyond that of the adjacent Al_2O_3 by 2.13 eV so a quantum well is formed where holes can be confined in. This analysis supports the observed hole trapping in the NPs.

Moreover, the endurance characteristic of the memory is analyzed by plotting the V_t of both programmed and erased states versus the number of program/erase cycles as shown in Fig. 7. The measurement was made up to 10^5 cycles at room temperature where a good V_t shift (2.9 V) is still present.

Additionally, the retention characteristic of the NPs is investigated by measuring the V_t shift vs. time at room temperature as shown in Fig. 8. The curve is extrapolated to 10 years where the memory cell exhibits a noticeable V_t shift of 2 V, which means a loss of 39.4% of the initial charge in 10 years [17]. The good retention of the memory cell is due to the good confinement of holes in the Si-NPs.

The retention characteristic can be further justified by calculating the stored holes lifetime. The stored holes in the Si-NPs must tunnel back through the 5-nm Al_2O_3 and 1-nm interfacial SiO_2 layer. The ground state energy of the holes confined in 2-nm Si-NPs is first calculated by adopting the following equation [30]:

$$E_0 = \frac{h^2\pi^2}{2m_0L^2}, \tag{5}$$

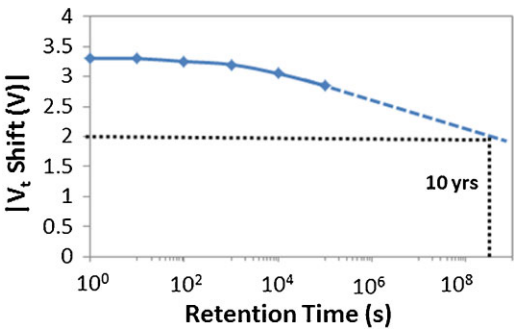

Figure 8 Measured retention time of the memory system at room temperature showing a good retention (>10 years).

where $\hbar$ is the reduced Plank's constant, m_0 is the hole effective mass, and L is the thickness of the Si-NPs. The resulting ground state energy is $E_0 = 192.1$ meV. The tunneling probability can be then approximated using Eq. (3) [30]:

$$T = 16\left(\frac{E_0}{V_0}\right)\left(1-\frac{E_0}{V_0}\right)e^{-2d\frac{\sqrt{2m_0(V_0-E_0)}}{\hbar}}, \tag{6}$$

where V_0 is the potential energy of the barrier and d is the thickness of the barrier [31]. The transmission probability is found by multiplying the tunneling probability through Al_2O_3 by the tunneling probability through the interfacial SiO_2 oxide and it is found to be $T = 2.078 \times 10^{-23}$. The attempt frequency can be estimated from $\upsilon = \frac{E_0}{2\pi\hbar} = 4.64 \times 10^{13}\ s^{-1}$, and the trap lifetime of a hole confined in Si-NPs between the barriers would be [30] $\tau = (\upsilon T)^{-1} \sim 33$ years. The results support the measured long retention characteristic (>10 years) of the memory structure with Si-NPs.

Finally, the electric field across the tunnel oxide is calculated using Gauss's law [29] and found to be 3.35 MV/cm at a gate voltage of 8 V. Lim et al. [32] have reported the transport mechanism in 5-nm ALD deposited Al_2O_3 on Si with respect to the value of the electric field across the tunnel oxide, and for $E_{ox} \geq 3.35$ MV/cm, the dominant charge emission mechanism is Fowler–Nordheim tunneling where holes tunnel through a triangular energy barrier into the tunnel oxide and then get swept by the electric field across the tunnel oxide into the charge trapping layer. Thus, the expected dominant holes emission mechanism in the demonstrated memory is Fowler–Nordheim tunneling at $E_{ox} \geq 3.35$ MV/cm.

4 Conclusion A 2-nm Si-nanoparticle charge trapping memory is demonstrated. The low-cost and simple memory structure showed a 3.3 V memory. This confirms that the 2-nm Si-NPs behave as holes trapping centers with high charge trapping density. The dominant hole emission mechanism is Fowler–Nordheim. Moreover, the memory cell showed low frequency dispersion between 10 kHz and 1 MHz C–V measurements which makes the use of 2-nm Si-NPs in such memory structure promising. Finally, the long retention time and the good endurance characteristic of the memory prove that Si-NPs are a good candidate for charge trapping layers in future low-cost nonvolatile memory devices.

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