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Lateral overgrowth of germanium for monolithic integration of germanium-on-insulator on silicon

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ABSTRACT

A technique to locally grow germanium-on-insulator (GOI) structure on silicon (Si) platform is studied. On (001) Si wafer, silicon dioxide (SiO_2) is thermally grown and patterned to define growth window for germanium (Ge). Crystalline Ge is grown via selective hetero-epitaxy, using SiO_2 as growth mask. Lateral overgrowth of Ge crystal covers SiO_2 surface and neighboring Ge crystals coalesce with each other. Therefore, single crystalline Ge sitting on insulator for GOI applications is achieved. Chemical mechanical polishing (CMP) is performed to planarize the GOI surface. Transmission electron microscopy (TEM) analysis, Raman spectroscopy, and time-resolved photoluminescence (TRPL) show high quality crystalline Ge sitting on SiO_2. Optical response from metal–semiconductor–metal (MSM) photodetector shows good optical absorption at 850 nm and 1550 nm wavelength.

1. Introduction

Ge shows great promise in electronic and optical applications. Its low optical bandgap of 0.66 eV allows it to absorb infrared (IR) light. With strain engineering, its optical bandgap can be further decreased to detect 1550 nm and longer wavelength light, which is crucial for optical telecommunication systems. With sufficient tensile strain Ge can become a direct bandgap material making light emission possible [1]. Its more symmetric and higher carrier mobilities also make Ge a strong candidate for high speed CMOS applications. To incorporate Ge based devices on a silicon (Si) based platform, integration of the two materials is needed. Hetero-epitaxial growth [2–4] has been actively studied and with the multiple hydrogen annealing at high temperature (MHAH) technique [4], high quality Ge films can be grown on Si. For monolithic integration, selective epitaxial growth has also been studied using SiO_2 as growth mask. With the help of aspect ratio trapping (ART), growth of high quality Ge films, which could be used for optical/electrical devices, has been demonstrated [5–7].

For high speed optical telecommunication, optical devices based on GOI are being studied [8]. Ge detectors made on epi-Ge films directly grown on Si suffer from slow optical responses because photo-generated carriers deep inside the Si substrate must travel a long distance to be collected at the metal electrodes at the top surface, thereby degrading bandwidth. By placing an insulating layer between Ge and Si, carriers generated within the thin Ge layer only contribute to the optical response and bandwidth can be drastically increased. With the use of GOI platforms, ~30 GHz bandwidth detectors have been demonstrated [8–10]. In

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addition, for Ge based FinFETs and gate all-around FETs, GOI is used to isolate the channel from the substrate [11,12].

Several different approaches have been studied for creating GOI platform. Wafer bonding provides a very high quality GOI, but the GOI cannot be monolithically integrated with Si substrate and the process cost is expensive [13–16]. Rapid melt growth (RMG) is an alternative approach, but due to the high melting temperature of Ge, the process is limited by the thermal budget and controlling Si diffusion into Ge is problematic [17–20]. Electrical and optical devices have been demonstrated on hetero-epitaxial grown Ge on thin silicon-on-insulator (SOI) [11,12] but the resulting GOI suffers from high density of threading dislocation and the resulting devices are affected by the underlying Si/Ge interface. Additionally, an SOI based GOI approach increases the overall cost of manufacturing due to the high price of SOI substrates.

Lateral overgrowth (LAT-OVG) is another promising approach for monolithic integration of GOI on a Si substrate [20]. ART, defect necking, and hydrogen annealing effectively suppress threading dislocations from the Si/Ge interface. Still, the resulting Ge crystal quality can be limited by the limited growth selectivity. If the selectivity is not high enough, during the growth, poly-crystalline Ge nuclei are formed on the GOI region [21]. Also, when the neighboring Ge crystals coalesce, voids are formed at the point of coalescence in the middle of the GOI region and this void limits further device applications on the resulting GOI [22].

In this paper, LAT-OVG technique for a GOI platform is studied. Suppressing poly-crystalline Ge nucleation due to the limited growth selectivity is studied and technique to eliminate the void is developed. By using optimized growth conditions for each of the seed layer growth, selective growth, and lateral growth steps, monolithic integration of high quality GOI without void and poly-crystalline nuclei is demonstrated. By separating the active GOI region from the Si/Ge growth interface and with help of ART, the Ge film quality is improved. We also demonstrate a metal–semiconductor–metal (MSM) photodetector integrated on this GOI platform to show the possibility of monolithic integration of Ge based optical devices on a Si substrate.

2. Process flow

A schematic process flow is shown in Fig. 1(a). Starting with a Si (001) substrate, thermal oxide is grown for the Ge growth mask. The growth window is defined by dry etching (Fig. 1(a1)). For better starting Si surface, bottom 20 nm of the oxide is wet etched using HF. The mask edges are aligned along $<110>$ directions. On this substrate, crystalline Ge is grown epitaxially. During the growth at low temperature (400 °C), multiple steps of hydrogen annealing are performed at 825 °C to anneal the defects. After the growth window is filled, Ge starts to grow laterally along the SiO_2 surface (Fig. 1(a2)). When neighboring Ge crystals coalesce with each other, $<100>$ directional growth perpendicular to the substrate surface becomes dominant and valleys are quickly filled (Fig. 1(a3)). CMP is performed to make the surface planar (Fig. 1(a4)). The resulting crystalline Ge film sitting on SiO_2 can be used for GOI applications.

For the Ge growth, after HF-last standard cleaning process, the sample is loaded into an Applied Materials Centura epitaxial reactor and the wafer is baked at 1000 °C in hydrogen (H_2) to remove Si native oxide. To ensure the high quality of a starting seed layer, a thin Si layer is grown selectively on the exposed Si growth windows using dichlorosilane (DCS). A 100 nm seed Ge layer is grown using 10 sccm of germane gas (GeH_4) at 30 T and low temperature (400 °C) for better surface coverage [23] for 300 s. Measured growth rate high temperature annealing is then performed under hydrogen ambient. This cycle is repeated twice

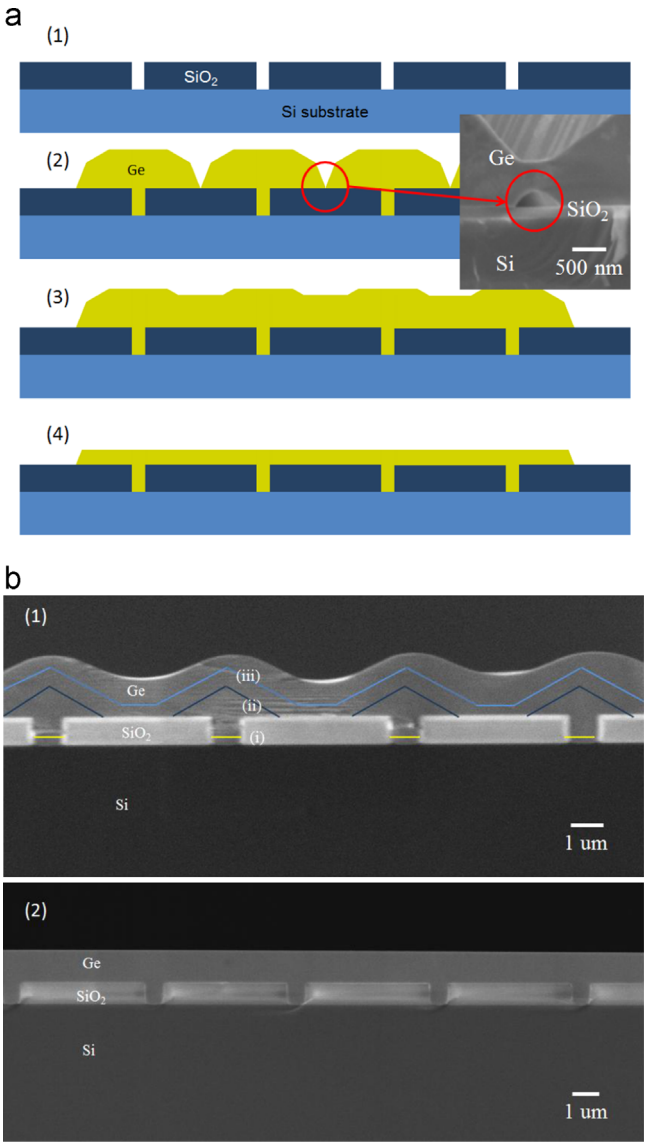

Fig. 1. (a) Process flow for LAT-OVG and (b) cross-sectional SEM. (a) Process flow: (1) thermal oxidation and growth window definition, (2) growth window filling, lateral growth, and coalescence, (3) gap filling, and (4) CMP. (b) Cross-sectional SEM: (1) (i) initial seed layer growth, (ii) growth window filling, (iii) lateral growth, and $<001>$ directional growth. Final high temperature (825 °C) annealing after $<001>$ directional growth rounds the facet shape. (2) Planarization by CMP. Growth window width is 500 nm, oxide thickness 900 nm, and oxide width 5 μm.

for better crystal quality. On this 300 nm thick seed layer, Ge is further grown under various conditions using germane.

3. Results and discussion

3.1. Growth selectivity and nucleation

When an incoming Ge species arrives and is adsorbed on the growth mask surface, it starts to diffuse along the surface. If the species meet nearby Ge epitaxial crystalline regions within a surface diffusion length, they add to the epitaxial growth. Otherwise, they start to form poly-crystalline nuclei.

Unlike the selective growth process, since the Ge layer on the insulator using LAT-OVG is used as an active region for device applications, it is crucial to control the growth selectivity in order to obtain a high quality GOI. SiO_2 and low pressure chemical vapor

deposition (LPCVD) silicon nitride (Si_3N_4) grown or deposited under different conditions were tried as growth masks. Unlike SiO_2, Si_3N_4 provides poor growth selectivity similar to Si selective growth [24]. Although low temperature silicon oxides (LTOs) do not provide decent selectivity, selectivity can be improved when the LTOs are densified at high temperature (higher than 1000 °C). Thermal oxides grown at temperature higher than 1000 °C give the best growth selectivity.

Although thermal oxide grown at 1100 °C provides decent selectivity, poly-crystalline Ge nuclei are formed on SiO_2 surfaces during relatively thick Ge growth required for LAT-OVG. Similar to LAT-OVG of Si [25], adding an etchant gas (HCl) can effectively suppress this nucleation as shown in Table 1. Adding HCl during the growth makes the lateral growth slower. For comparison, the oxide thickness is set to 300 nm, growth window width to 500 nm and the oxide width to 5 μm. Nuclei density is measured when the lateral growth covers the 5 μm wide oxide completely. Without HCl, it took 1000 s, with 40 sccm 1200 s, with 80 sccm 2000 s, and with 160 sccm, 2800 s is needed. The nuclei density is counted at ~50 μm away from the growth opening, so the actual nuclei density within the active GOI region between growth windows should be much lower.

Table 1
Nucleation density on SiO_2.

Sample	GeH_4 (sccm)	HCl (sccm)	Nucleation density (/100 μm^2)
a	40	0	> 100
b	40	40	35
c	40	80	25
d	40	160	5

Growth temperature is set to 600 °C, and pressure to 30 T.

3.2. Void formation and elimination

During the lateral growth phase, the growing Ge crystal tends to have negative slope at the growth front to minimize the surface energy. When neighboring Ge crystals coalesce with each other, this reentrant growth region leaves a void. Once coalescence happens, no further Ge species can reach this void region, so this void remains embedded as shown in Fig. 1(b).

To eliminate these voids, various experiments using different growth conditions are performed. The overall shape of the Ge crystal during the growth is determined by the relative growth rates of different crystal planes. For selective Ge growth, bounding crystal planes are <100>, <111> and <311>, and their relative growth speeds can be adjusted by varying the growth temperature, growth window stripe pattern direction, and etchant gas (HCl) flow. By changing the shape of the growing Ge crystal, the void size can be engineered, and at certain conditions, the void can be completely eliminated. While the growing Ge crystal is filling the growth window,

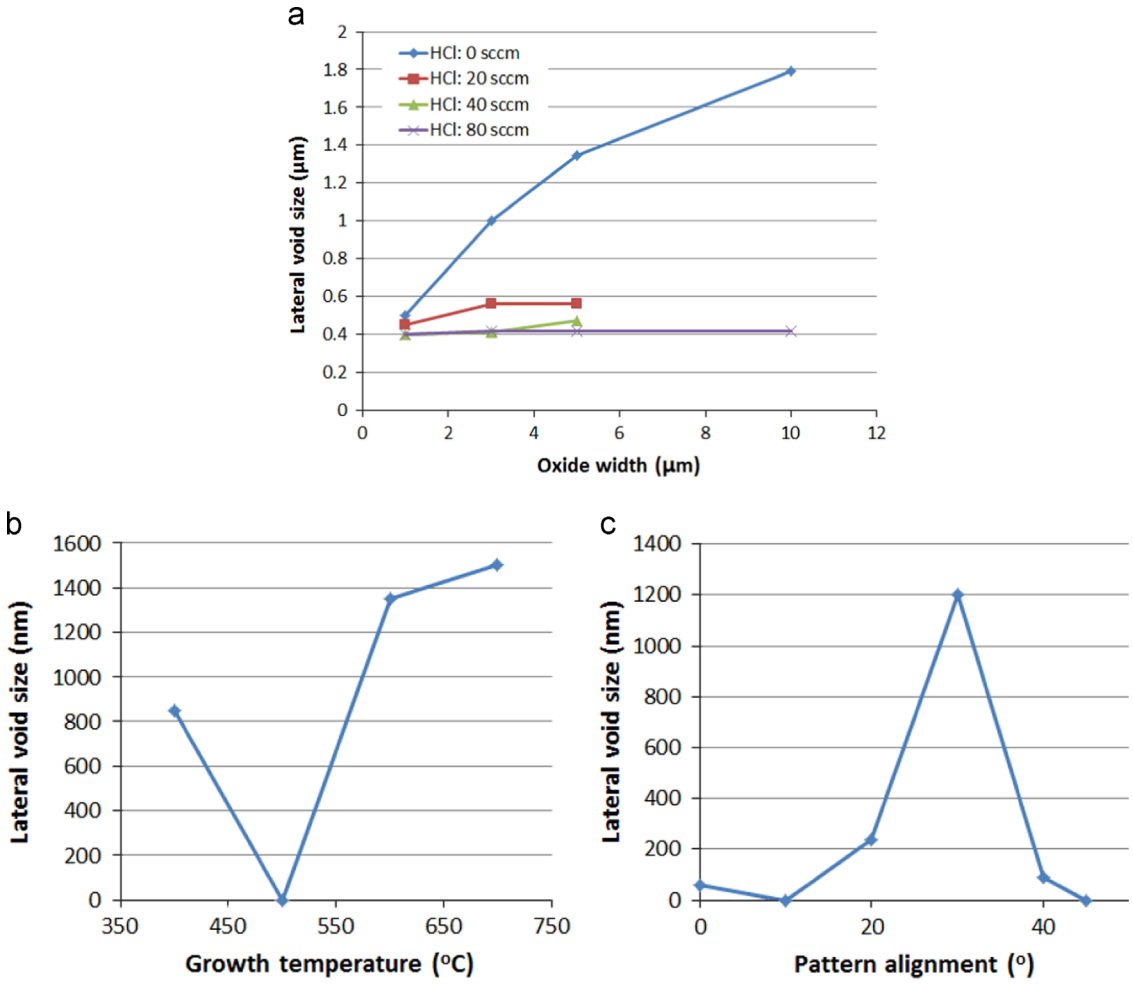

Fig. 2. Engineering lateral void size. (a) Lateral void size vs. oxide width. Growth temperature is set to 600 °C. (b, c) Lateral void size under various growth conditions. Oxide width is fixed to 5 μm, and no HCl gas is used. Growth time is fixed to 4000 s for coalescence. The void size is measured by cross-sectional SEM. (b) Lateral void size vs. growth temperature. Growth window pattern is aligned along the <110> direction. (c) Lateral void size vs. growth window stripe pattern alignment. 0° alignment means the pattern is aligned along the <110> direction, and 45° means <100> direction. Growth temperature is set to 600 °C, and pressure 30 T.

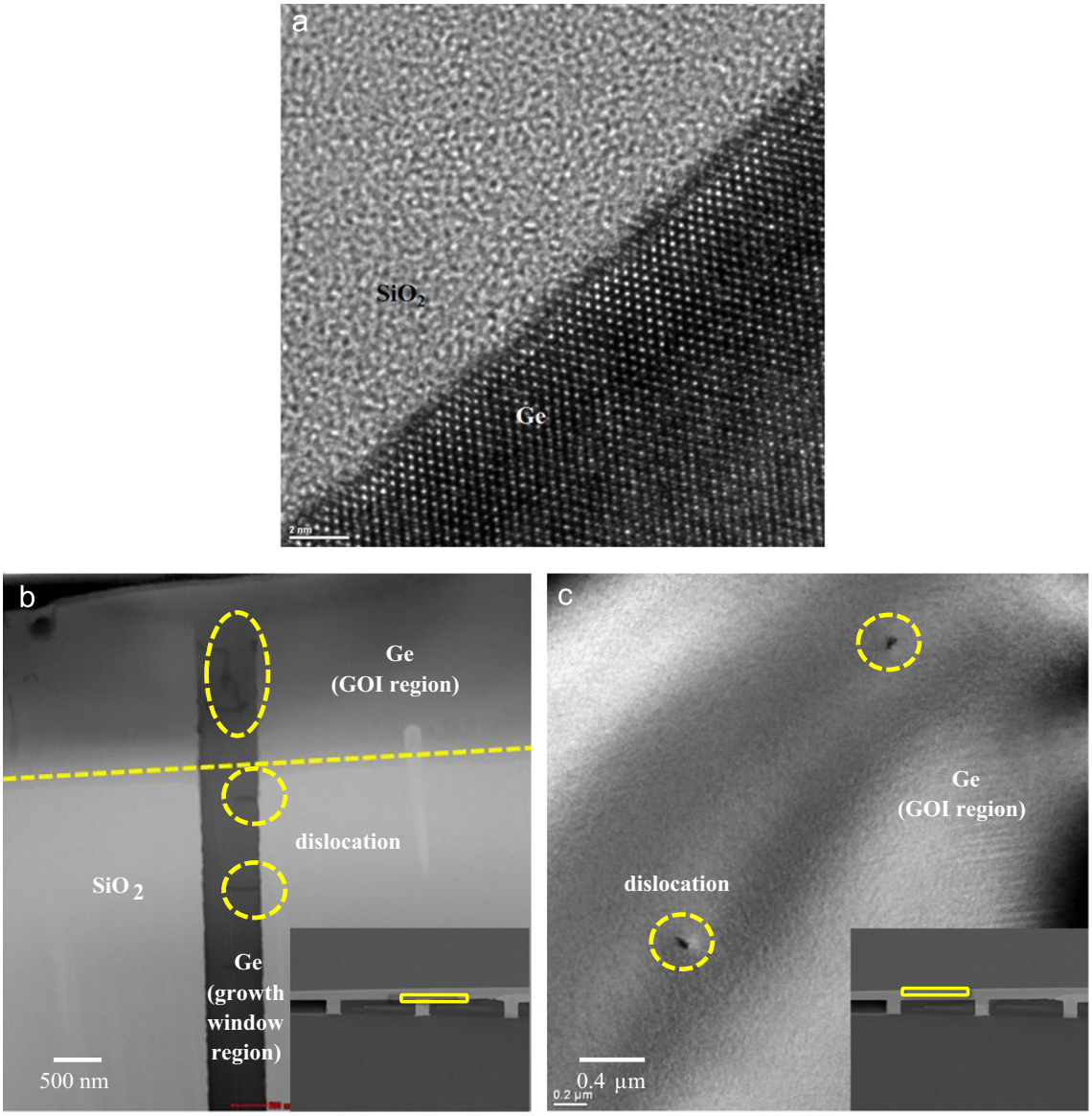

Fig. 3. Cross-sectional and plan-view TEM analysis. Growth window width is 0.5 μm and oxide width is 5 μm. Oxide thickness is 900 nm. (a) Cross-sectional TEM in GOI region. (b, c) Plan-view TEM. (b) Top of the growth window. Defects propagating along $<110>$ direction are seen. TDD is 8×10^{7} cm^{-2}. (c) GOI region. Threading dislocations are marked with circle. TDD is $1–3\times10^{6}$ cm^{-2}. Insets in both figures show the region of TEM analysis.

Table 2
Raman spectroscopy: peak position and FWHM.

	Bulk Ge	epi-Ge	LAT-OVG GOI
Peak position (cm^{-1})	299.950	299.059	299.229
FWHM (cm^{-1})	4.371	4.429	4.382
Strain (%) [33]	–	0.231	0.187

Un-patterned epi-Ge is 1.5 μm thick, and LAT-OVG is done on 900 nm thick thermal SiO_2 growth mask and GOI thickness is 600 nm.

the reentrant growth region at the growth front cannot be formed. The undercut forms and develops during the lateral growth. In the beginning, the undercut becomes bigger as the lateral growth proceeds and later saturates. As a result, with a relatively narrow oxide growth mask, the lateral void size increases with increasing oxide width and saturates with a wider oxide (Fig. 2(a)). For lateral void size measurement for each growth condition, oxide width is fixed at 5 μm and growth window opening is fixed at 3 μm. The measured void sizes for different growth conditions are shown in Fig. 2. Several process conditions which can eliminate the void are found (Fig. 2(b)–(c)).

3.3. LAT-OVG for GOI

By carefully choosing growth conditions and parameters affecting nucleation and void formation, an optimal LAT-OVG recipe for GOI can be designed. For ART, oxide thickness is set to 900 nm and the growth window width 500 nm. Oxide width, which is the resulting GOI width, is set to 5 μm (Fig. 1(b)), with resulting local oxide coverage of 91%. The overall growth process can be divided into three steps: (1) seed layer growth, (2) growth window filling and initial lateral overgrowth, and (3) lateral overgrowth and coalescence. For the seed layer growth, the primary concern is Ge islanding. During this first step, no etchant gas is used since nucleation on the oxide surface is negligible due to the small target thickness and due to short growth time. Ge is grown at lower temperature (400 °C) for better nucleation on the surface of Si [26].

Lower temperature growth also helps to improve the growth selectivity [27]. For the second step, growth window filling, primary concerns are Ge crystal quality and poly-Ge nucleation on SiO_2. The growth temperature is raised to 600 °C and etchant gas is added to suppress nucleation. To ensure high growth selectivity, 40 sccm of GeH_4 is flown with 160 sccm of HCl at 30 T (Table 1). After 1000 s, complete filling of the growth window and 1.5 μm of additional lateral growth is achieved. Two steps of high temperature annealing are incorporated to increase the crystal quality. For the lateral overgrowth and coalescence step, eliminating the void becomes the primary concern. Growth conditions which can eliminate the void (Fig. 2) are needed at this stage. While maintaining the pressure at 30 T, the growth temperature is set to 500 °C for the void elimination (Fig. 2). To maintain decent growth selectivity, GeH_4 flow is also reduced to 10 sccm. The growth speed of $<311>$ growth plane is 30 nm/min at this condition. To ensure the coalescence over the 5 μm wide oxide strip, growth is done for 1200 s. After the coalescence, high temperature (825 °C) hydrogen annealing is followed to enhance Ge migration and anneal dislocations which could have been generated at the coalescence point. Further growth is done at 600 °C to make $<001>$ directional growth dominant. At this stage, the SiO_2 surface is completely covered with Ge and nucleation cannot occur. GeH_4 flow is now raised to 20 sccm for faster growth. Under this condition, the measured $<001>$ directional growth speed is 200 nm/min and the valley at the center of each GOI region is quickly filled within 300 s. For better crystal quality, final high temperature annealing is performed at 825 °C (Fig. 1(b)).

3.4. CMP and planarization

Fig. 1(b1) shows a cross-sectional scanning electron micrograph (SEM) image. Despite of surface planarization due to the valley filling and the surface migration during high temperature annealing, macro-scale height differences still exist because coalescence does not happen exactly at the same time along the long growth front and because the geometry of the growth window pattern underneath may vary. To achieve a planar surface, CMP is performed. GnP Poly-400L CMP system with Ultra-Sol S10 slurry (70 nm colloidal silica) is used. Measured polishing rate of Ge on the GOI is 100 nm/min. After CMP, the surface RMS roughness is decreased down to 0.6 nm (Fig. 1(b2)).

3.5. Quality of GOI

LAT-OVG separates the active GOI device regions from the defective Si/Ge interface and benefits from ART and defect necking [28]. Hence Ge crystal quality in GOI can be improved as compared to blanket growth with the same thickness. Cross-sectional TEM (Fig. 3(a)) shows very high quality Ge grown on SiO_2.

Threading dislocation density (TDD) is obtained by plan-view TEM (Fig. 3(b)–(c)) and atomic force microscopy (AFM). TDD values from two different regions are measured: at the top of the growth window (Fig. 3(b)), and on the GOI region (Fig. 3(c)). At the top of the growth window region, 900 nm above the Si/Ge interface, measured defect

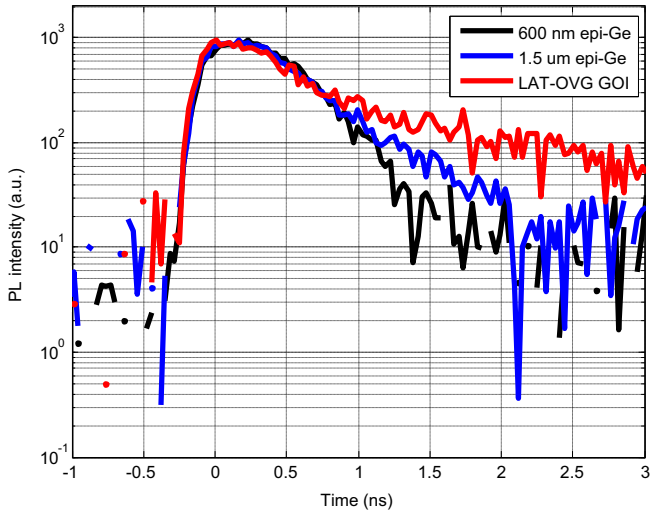

Fig. 4. Time-resolved photoluminescence from 500 nm and 1.5 μm un-patterned epi-Ge and 600 nm thick GOI on 900 nm SiO_2 from LAT-OVG.

Table 3
Minority carrier lifetime from TRPL.

	600 nm epi-Ge (Bulk growth)	1.5 μm epi-Ge (Bulk growth	LAT-OVG GOI
TDD (cm^{-2})	3×108*	2×107*	$1–3 \times 106$
Lifetime (ns)	0.239	0.615	1.767

LAT-OVG is done on 900 nm thick thermal SiO_2 growth mask and GOI thickness is 600 nm.

* TDD numbers for un-patterned epi-Ge are from previous study [26].

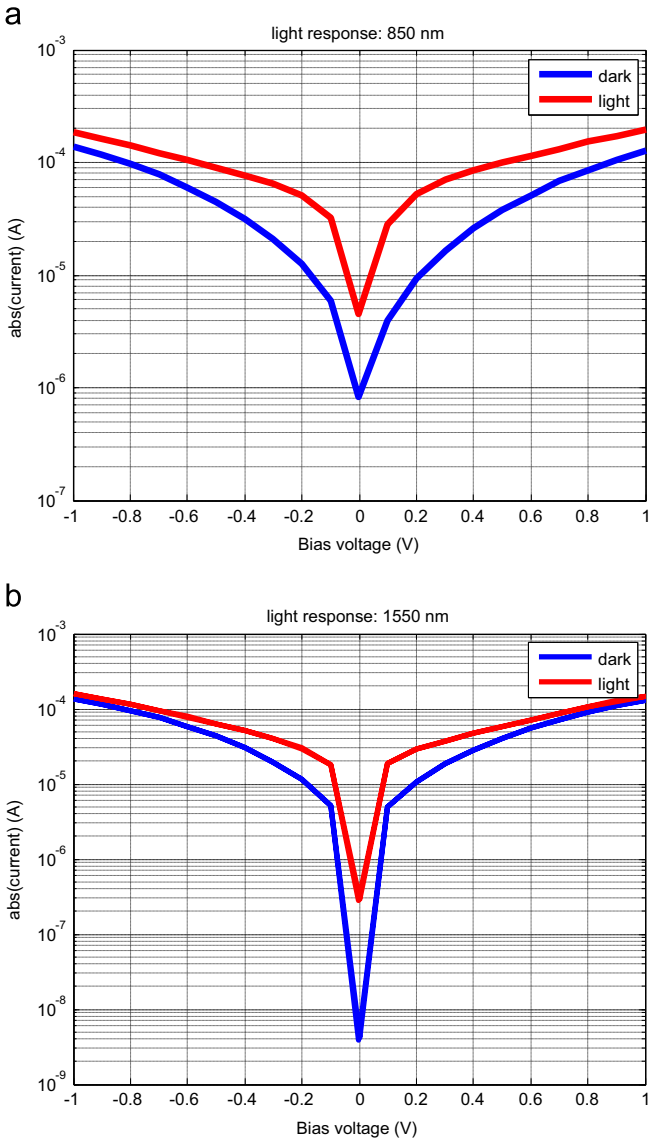

Fig. 5. LAT-OVG MSM light response. (a) wavelength: 850 nm, laser power: 540 μW and (b) wavelength: 1550 nm, laser power: 100 μW.

density is $8\times10^7\,cm^{-2}$. This number is not so different from previously reported numbers on bulk growth with the same thickness (900 nm) [26,29] and comparable to the selective epitaxial growth without ART (Fig. 3(b)). On the other hand, TDD measured on a 600 nm thick GOI region drops to $1–3\times10^6\,cm^{-2}$ (Fig. 3(c)). This number is more than $10\times$ improvement over the previously reported value from bulk growth [24,26] and shows that TDD is effectively suppressed by defect necking.

Raman spectroscopy is used to measure the in-plane strain (Table 2). Both un-patterned epi-growth and LAT-OVG give biaxial tensile strain [30–32], but when compared to the un-patterned epi-growth, strain level in LAT-OVG is smaller (Table 2) [33]. Full width half maximum (FWHM) also confirms the improvement in Ge crystal quality by employing LAT-OVG.

TRPL [34] is used to measure minority carrier lifetime in LAT-OVG GOI. Results using time-correlated single-photon counting technique are shown in Fig. 4 and Table 3. Compared to the un-patterned epi-growth with the same thickness (600 nm), LAT-OVG GOI shows more than $7\times$ improvement in minority carrier lifetime. Since threading dislocations act as acceptor-like traps and limit minority carrier lifetime [35,36], lower threading dislocation density is believed to be the main reason for this improvement. $\sim3\times$ improvement in minority carrier lifetime is observed in LAT-OVG GOI when compared to un-patterned growth Ge with same growth distance from Si/Ge interface (1.5 μm).

Since GOI-based photodetectors monolithically integrated on Si platform using bulk epi-growth on SOI suffered from large dark current mainly due to the high TDD [6,37,38], this low TDD number and subsequent results are very encouraging for further optoelectronic device applications.

3.6. Photoresponse

For this platform to be useful for optical interconnects applications, a good optical response at wavelengths of 850 nm and 1550 nm is crucial [39]. To demonstrate the optical response, simple metal–semiconductor–metal (MSM) photodetector is made on LAT-OVG GOI. Thickness of the oxide growth mask is kept 900 nm and the thickness of the GOI 600 nm. Active region is defined by dry etching to isolate the devices from the growth window area which is defective. On this GOI mesa, lateral MSM is fabricated. For the metal contact, 20 nm chromium followed by 200 nm gold is used. Distance between the metal contacts is 5 μm. 850 nm and 1550 nm lasers are used and the device is illuminated from the top. Current–voltage (I–V) characteristics with and without light are shown in Fig. 5. Though dark current is high due to the Fermi level pinning, I–V characteristics show optical absorption of LAT-OVG GOI at 850 nm and 1550 nm wavelengths, confirming that this platform can be used for optical interconnects.

4. Conclusion

The influence of growth conditions on LAT-OVG is studied. An optimal recipe for LAT-OVG is designed by using different process conditions during different steps of the growth. Initial Ge seed layer growth is done at a low temperature (400 °C) which provides better coverage. Hydrogen annealing is done at high temperature (825 °C) after the seed layer growth. This cycle is repeated several times for a better quality seed layer deposition. On this seed Ge layer selective Ge growth is done to fill the growth window, with high HCl gas flow used to minimize nucleation on the oxide. During the lateral growth phase, growth conditions are optimized to eliminate any void at the intersection of the two growth fronts. After coalescence, the HCl gas is turned off since nucleation suppression is no longer needed. After the initial valleys are filled by dominant $<100>$ growth, CMP is done for further planarization. High quality crystalline Ge on SiO_2 is observed by cross-sectional TEM. Low TDD of $1–3\times10^6\,cm^{-2}$ is measured from plan-view TEM analysis. Raman spectroscopy is used to evaluate the strain level. Just like the bulk epi-growth, 0.20% of residual biaxial tensile strain is observed. MSM light response confirms good light absorption at 850 nm and 1550 nm wavelengths and this GOI platform can be used for optical interconnects.

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