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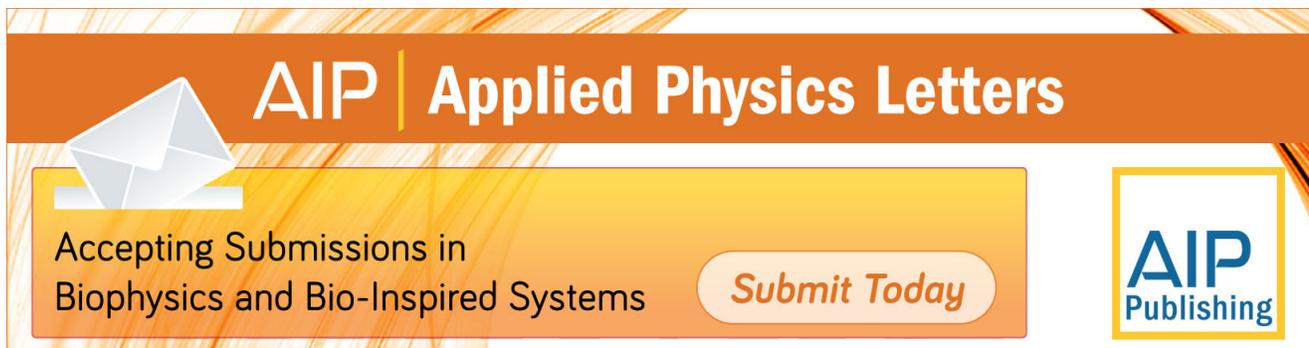
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Comparison of electron and hole charge-discharge dynamics in germanium nanocrystal flash memories

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Electron and hole charge and discharge dynamics are studied on plasma enhanced chemical vapor deposition grown metal-oxide-silicon germanium nanocrystal flash memory devices. Electron and hole charge and discharge currents are observed to differ significantly and depend on annealing conditions chosen for the formation of nanocrystals. At low annealing temperatures, holes are seen to charge slower but to escape faster than electrons. They discharge slower than electrons when annealing temperatures are raised. The results suggest that discharge currents are dominated by the interface layer acting as a quantum well for holes and by direct tunneling for electrons. © 2008 American Institute of Physics. [DOI: 10.1063/1.2835455]

Nanocrystals (NCs) of Silicon (Si) and Germanium (Ge) in silicon based dielectric materials have attracted a lot of attention in recent years for applications in opto- and micro-electronics. NCs can be formed, typically, by ion implantation or plasma enhanced chemical vapor deposition of semiconductor rich dielectrics and post annealing. Both Si and Ge NCs are being considered for applications in flash memories and they have been studied extensively.¹

In order to study charge and discharge dynamics of carriers in nanocrystal memories, conventional floating gate models have been applied by De Salvo *et al.*² and later modified to include the discrete nature of the charges.³ It is well known that direct tunneling dominates in thinner oxides whereas thicker oxides require Fowler–Nordheim (FN) tunneling. Results of hydrogen annealing experiments in Si NCs pointed to the role of traps in the NCs during charging and discharging, and modeled by Campera and Iannaccone⁴ Charge retention at deep traps in Ge NCs was also observed.^{5,6} Seemingly long retention times suggested that carrier discharge occurs through direct tunneling in the absence of interface states.⁷ However, long retention times are meaningful only when write times are short. Truly long hole retention times were found in chemical vapor deposition (CVD) grown Ge NCs with Si precursors without postannealing.⁸ Theoretically, Ge NCs are thought to be better suited for data retention due to its smaller band gap compared to Si. Recently, it was also suggested⁹ that hole storage in SiGe NCs has important advantages in terms of retention of carriers. However, none of these studies considered the role of interface layers, which should be included in any realistic model of NC memory devices.

In Ge NC formation processes where post annealing is required, typical temperatures used range from 600 to 800 °C for the formation of Ge NCs. Since Ge is a fast diffuser in SiO₂, formation of Ge NCs is often accompanied by diffusion of Ge into the SiO₂/Si interface even at relatively low temperatures. Considering that the tunnel barrier in a flash memory is only a few nanometers thick, it is

hard to avoid diffusion of Ge under these conditions. The presence of Ge at the interface creates an interface layer, which has to be taken into account in any analysis of flash memories. In this work, we present experimental results that compare charging and discharging dynamics of electrons and holes in Ge NC metal-oxide-semiconductor (MOS) capacitors fabricated by plasma enhanced CVD (PECVD) with postannealing and discuss the validity of assumptions about dominant carrier discharge mechanisms. Trilayer MOS capacitor structures carrying Ge NCs as charge storage medium has been studied by capacitance-voltage (CV) spectroscopy. Electron and hole storage and escape have been characterized experimentally. The results point to the importance of the interface layer due to Ge diffusion to the SiO₂/Si interface.

The samples were grown using a parallel-plate-type PECVD reactor (PLASMALAB 8510 °C). Germanosilicate films were grown at 350 °C, in a pressure of 1 Torr and rf power of 10 W at a frequency of 13.56 MHz, applied to plates with a diameter of 24 cm using GeH₄ as the precursor. Trilayer structures consist of a 4 nm thick thermal oxide followed by a 10 nm thick Si_{0.6}Ge_{0.4}O₂ layer [as determined by x-ray photoelectron spectroscopy (XPS) characterization], capped with a 15 nm thick PECVD oxide. Annealing was done at temperatures of 650–850 °C for duration of 5 min under nitrogen environment. The samples were studied by cross sectional transmission electron microscopy (TEM) (not shown) and nanocrystal size distributions and areal densities were inferred. It is also observed that, for the fixed duration of annealing, samples annealed at 850 °C show precipitation of Ge to the silicon substrate interface as discussed elsewhere.¹⁰ The charge and discharge currents of NCs can be calculated separately assuming FN tunneling from the substrate to the NC layer during charging and direct tunneling during discharge.¹¹ Diffusion of Ge toward the interface, however, complicates the situation. The possibility of thin homogeneous and inhomogeneous alloy layers forming at the interface may lead to trapping and/or trap assisted tunneling which is especially important during retention. Since charge and discharge currents are dependent on a large number of

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parameters, it is hard to distinguish unambiguously these multiple mechanisms from the measurement and analysis of only the discharge current and single carrier type. However, comparison of charge and discharge currents for electrons and holes provides a greater contrast if the dominant discharging mechanism is not direct tunneling. One would expect to observe increased discharge rates if trap assisted tunneling during discharge is dominant. On the other hand formation of alloy islands or quantum wells at the interface may also inhibit discharge. In order to measure charge and discharge currents, we use a modified CV spectroscopy setup, where a feedback loop is used to measure flatband voltage shifts before and after applied pulses or during retention. The cumulative flatband shift is proportional to the total deposited charge after a number of write pulses and is given by¹²

$$\Delta V_{FB} = \frac{qn_{nc}}{\epsilon_{ox}} \left(t_{cox} + \frac{\epsilon_{ox} t_{nc}}{2\epsilon_{Ge}} \right), \quad (1)$$

where q is the electronic charge, t_{cox} is the control oxide thickness, t_{nc} is the average diameter of the NCs, and ϵ 's are the dielectric constants of respective materials. The charging current is assumed to be due to FN tunneling. The charging current density then becomes¹³

$$J_c = \frac{AF_{tox}^2}{V_B} \times \exp\left(-\frac{BV_B^{3/2}}{F_{tox}}\right), \quad (2)$$

where $A = q^2 m_{Si} / 16\pi^2 m_{ox} \hbar$, $B = 2\sqrt{8m_{ox}q} / 3\hbar$, F_{tox} is the tunnel oxide field during charging, m_{ox} is the tunnel effective mass, and V_B is the barrier height between the oxide and the substrate. The differential charges deposited per unit area $d\sigma$ in a time interval $d\tau$ can be calculated through $d\sigma = p_c D_t J_c(F_{tox}) d\tau$, where p_c is the average capture cross section and D_t is the available density of final states. The capture probability may depend on NC shape and $D_t \approx N_{NC}$ is the NC areal density. Similar studies of charge and discharge current have been recently reported.¹⁴ It is well known that, as the storage layer is saturated with carriers, the flatband shift reaches a maximum value in both conventional and NC flash memories.¹⁴ We, therefore, consider only small flatband voltage shifts for comparison of charge and discharge dynamics.

The flatband voltage shift measured between repetitive $d\tau = 25$ ms write pulses of varying voltage values are recorded.¹¹ Noting that, the derivative of the flatband voltage shift divided by pulse duration gives the charge current density, we plot the charging current per nanocrystal in Fig. 1. It is seen that, for small charging currents, charging current increases monotonically for n and p type samples, in a manner proportional to the NC density, consistent with TEM data indicating average diameters of ~ 3.1 and ~ 7.4 nm and densities of 3.8×10^{12} and $8.0 \times 10^{11} \text{ cm}^{-2}$ for samples annealed at 700 and 800 °C, respectively. It is observed that, for voltage pulse amplitudes of less than 4 V, the charge currents for electron and holes are roughly on the same order of magnitude, electrons tunneling faster by less than a factor of three than holes. This is understood by noting that hole barrier is greater when SiO₂ is used as the tunnel dielectric. The discharge currents have been measured in the same setup by monitoring the flatband voltage shift as a function of time. The derivative of the flatband voltage shift is calculated numerically and plotted as a function of time in Fig. 2. The

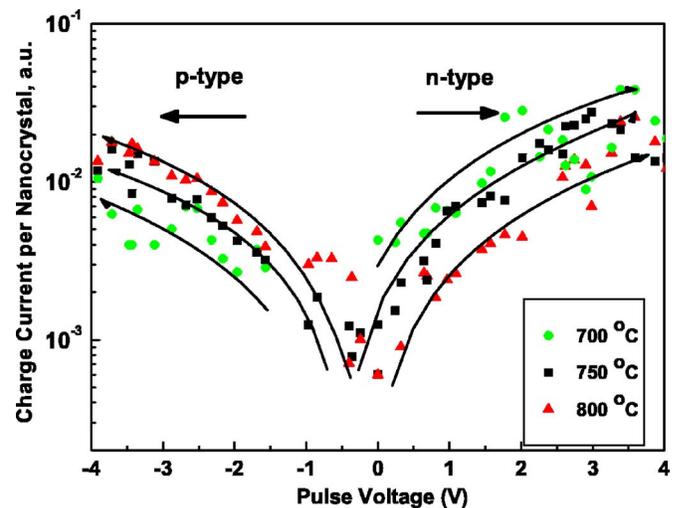


FIG. 1. (Color online) Experimental data of charging of n (right) and p (left) type capacitors. Charging currents as a function of charge voltage are measured for samples annealed at 700–800 °C.

flatband voltage shifts are with respect to the uncharged devices, therefore, the flatband shift due to surface pinning modification is already taken into account. It is seen that, the discharge currents of holes are larger than that of electrons for a similar flatband voltage shift at low annealing temperatures. However, as the annealing temperature is raised, hole escape rates drop below those of the electrons, the difference becoming larger at higher the annealing temperatures.

As the direct tunneling current is normally expected to be weak, surprisingly high hole discharge current at low annealing temperatures suggests that hole discharge dynamics are dominated by other mechanisms than direct tunneling such as trap assisted tunneling. On the other hand, samples annealed at higher temperatures show very low escape times for holes. This suggests that there is significant trapping of holes during the discharge phase. This could be understood by considering two factors that come into play at higher annealing temperatures. First, as the temperature is raised, nanocrystal sizes increase which in turn results in a higher energy barrier for holes bound at quantum states of the nano-

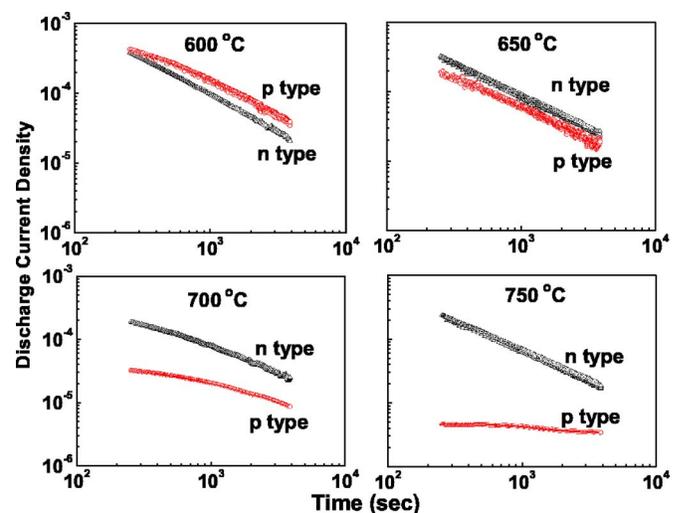


FIG. 2. (Color online) Discharge current densities as a function of time for n and p type devices. The holes decay faster than the electrons for samples annealed at low temperatures whereas they decay much slower for samples annealed at higher temperatures.

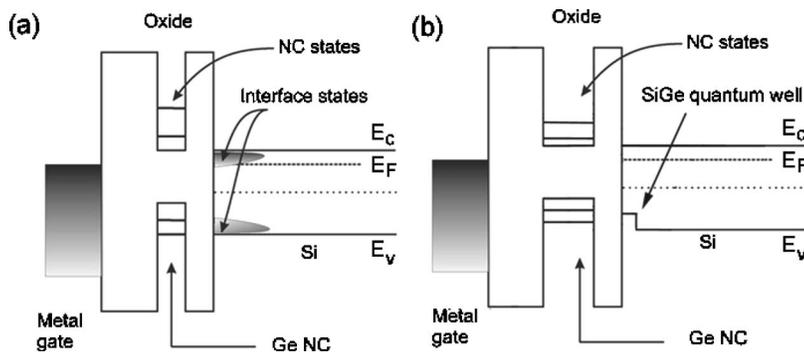


FIG. 3. Band structure of Ge nanocrystal MOS capacitor. (a) annealed at low temperatures and (b) annealed at high temperatures. Note the effect of quantum well at the interface and the increased nanocrystal size.

crystal. Second, the diffusion of Ge to the interface should result SiGe alloy formation which constitutes a quantum well. This results in more homogenous layer with less interface states. In addition, on their way to the substrate, holes encounter to the substrate encounter the quantum well and are trapped at the bound states of the quantum well. Increased annealing temperatures result in longer diffusion lengths for Ge, hence, wider quantum wells and larger barriers for holes trapped in the quantum well.

The results are summarized in the schematic band diagram for electrons and holes in Fig. 3. Note that at low annealing temperatures, Ge atoms diffusing to the interface do not form a homogenous layer. However, they create significant amount of interface trap states in the band gap of Si near the valence band edge lie energetically close to the confined states of holes in Ge NCs in contrast with electron confined states, which are above the conduction band edge. It can be argued that, both the valence band states and the presence of large number of traps within the silicon band gap result in an increased discharge current, mainly due to trap assisted tunneling of holes, [Fig. 3(a)]. As the annealing temperature is raised, the energy band diagram is modified by the presence of a thin quantum well at the oxide/Si interface and the presence of larger nanocrystal sizes, [Fig. 3(b)]. It should be noted that, introduction of Ge into Si does not change the conduction band appreciably while the valence band is raised.¹⁵ This is the reason for the different behavior of holes than electrons.

In conclusion, we have studied charge and discharge dynamics of both electrons and holes in PECVD grown and post annealed Ge NCs MOS capacitors. We find that in contrast with idealistic models of such devices, hole retention times are actually shorter than electron retention times for samples annealed at low temperatures. We suggest that the observed reduction of hole retention times is due to interface

traps states. However, formation of a Ge rich alloy at the interface with high temperature annealing results in longer retention times, which is promising for actual device operations. These observations emphasize the importance of proper interface engineering for Ge NCs memory devices.

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