Investigation of high frequency performance limit of graphene field effect transistors

Ercag Pince and Coskun Kocabas[a)]
Department of Physics, Advanced Research Laboratories, Bilkent University, 06800 Ankara, Turkey

(Received 2 September 2010; accepted 6 October 2010; published online 26 October 2010)

Extremely high field effect mobility together with the high surface coverage makes graphene a promising material for high frequency electronics application. We investigate the intrinsic high frequency performance limit of graphene field effect transistors limited by the charge impurity scattering. The output and transfer characteristics of graphene field effect transistors together with the high frequency performance are characterized as a function of impurity concentration and dielectric constant of the gate insulator. Our results reveal that graphene transistors could provide power gain at radio frequency band. © *2010 American Institute of Physics*.
[doi:10.1063/1.3506506]

Recent advances of chemical vapor deposition of graphene on large area substrates[1–3] stimulate a significant research effort searching for new applications of graphene in the field of unusual electronics such as macroelectronics.[4,5] Graphene can function as an effective semiconductor[6,7] or a transparent conducting coating[1,8–10] for large area displays and photovoltaic devices. Recent developments in scaling of graphene films open up new opportunities for flexible electronics.[1] Extremely high field effect mobility of graphene together with the large area deposition process,[2] could provide alternative solutions for the challenges of traditional organic materials. Operation at radio frequencies is one of the main challenges of the organic based field effect transistors owing to the poor field effect mobilities of organic semiconductors. Therefore radio frequency analog electronics could be an immediate high-end application of graphene transistors.[11]

Although high frequency analog electronics is a well established field for inorganic semiconducting materials, the effects of unusual transport properties of monoatomic graphene sheets at high frequencies are widely unknown. Recent experimental studies show several demonstrations of graphene and carbon nanotube arrays for high frequency operation.[12–15] Cut-off frequencies of 10 GHz for carbon nanotube arrays[14,16,17] and 100 GHz for graphene[13,18] have been achieved. Using critical design considerations, these values can be advanced by orders of magnitude. There is little in the literature that provides a simple, yet quantitative model to analyze the critical design considerations of radio frequency operation of graphene based field effect transistors. This work is aiming to develop an analytical model to design a graphene based rf (radio frequency) transistors based on diffusive transport governed by the charged impurity scattering.

A schematic representation of a model rf transistor is shown in Fig. 1(a). The transistor consists of a graphene layer printed on an insulating substrate (e.g., quartz or sapphire). The source and drain electrodes are formed on the graphene layer. A thin layer of dielectric material functions as a gate dielectric for the field effect transistor configuration. The gate electrode is formed on top of the gate dielectric. For the model, the dielectric thickness is 50 nm and the channel length and width are 1 μm.

Here, we consider the transport mechanism governed by the charged impurity scattering owing to the presence of the charged impurities on the substrate and the gate dielectric. The dielectric constant of the surrounding medium (gate dielectric and substrate) controls the effects of the impurity charges on the graphene layer. High-k dielectric materials (e.g., HfO_2) concentrate the electric field into the dielectric material and reduce the formation of residue charges on the graphene layer. Fang *et al.*[19,20] confirmed the effect of the charge screening on the charge mobility of the graphene.[20] Recent experimental results also agree with charge mobility lowering of graphene device by increasing charged impuri-

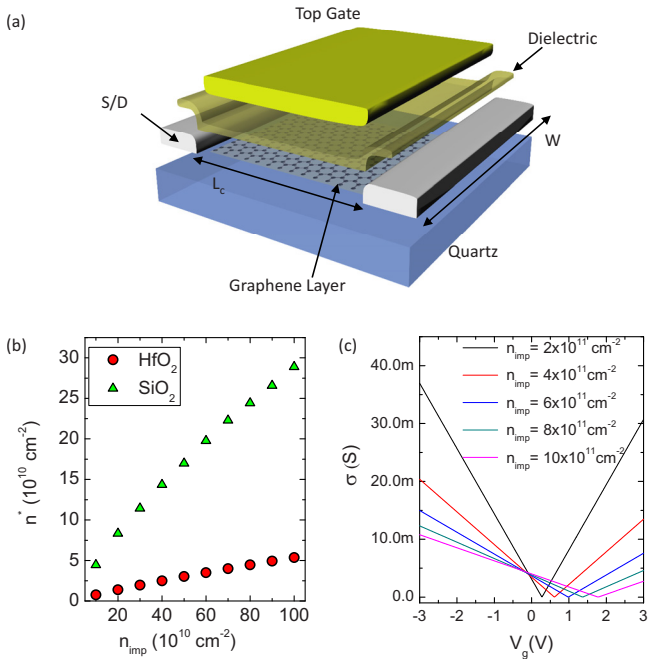

FIG. 1. (Color online) (a) Layout of a graphene based radio frequency transistor with a channel length L_c and channel width W. (b) The calculated residual charge concentration n^* as a function of charged impurity concentration n_{imp} for two different dielectric material HfO_2 and SiO_2. (c) The conductivity of graphene layers as a function of gate voltage. The charged impurity concentration is scanned from 2×10^{11} to 10×10^{11} cm^{-2}.

[a)]Author to whom correspondence should be addressed. Electronic mail: ckocabas@fen.bilkent.edu.tr. Tel.: +903122901965.

ties with potassium doping.[21] For the top gate configuration, both substrate and the gate dielectric determine the effective dielectric constant. Therefore, the substrate should have high dielectric constant or has to be coated with high-k material, such as HfO_2. A quartz wafer coated with a thin layer of HfO_2, grown by atomic layer deposition, could be a good substrate for graphene based rf transistors.

In the present analysis of the radio frequency devices we consider a self-consistent transport model developed by Adam *et al.* based on a charged impurity scattering. This model explains the most of the observed electrical behavior of graphene sheets, e.g., nonuniversal minimum conductivity and ultrahigh mobility of suspended graphene layers. The beauty of the model is that it requires only a few empirical parameters, density of charged impurities and the distance between the impurity and graphene layer and the dielectric constant of the surrounding medium. The distance of charged impurities between graphene is effectively located around 0.1–1 nm from the graphene sheet.[22]

We have analyzed the frequency response of graphene devices in three steps. First, we have used the self consistent model[23] to calculate the residual charge concentration n^* on the graphene layer [Fig. 1(b)]. After calculating the conductivity from the residual charge concentration, then we calculated the drain current at a given bias condition using a two-dimensional field effect transistor (FET) model. Scanning the gate and drain bias voltages we obtained the transfer and output curves of the device. Finally using the outcome of the device model we calculate the transconductance and associated cut-off frequency of the devices.

The residual charge concentration on graphene layer n^* depends on the charge impurity concentration and the dielectric constant of the gate dielectric and the substrate. Figure 1(b) shows the graph of residual charge concentration n^* as a function of charged impurity concentration n_{imp} for two different dielectric material HfO_2 and SiO_2. SiO_2 provides about six times more residue charges on graphene layer than HfO_2 owing to the low dielectric constant. Having calculated the residual charge concentration, we have calculated the conductivity of the graphene layer as a function of gate voltage by Eq. (1).[23]

$$\sigma(n-\bar{n}) = \begin{cases} \dfrac{20e^2 n^*}{h n_{\text{imp.}}} & \text{if} \quad n-\bar{n} < n^* \\ \dfrac{20e^2 n}{h n_{\text{imp.}}} & \text{if} \quad n-\bar{n} > n^* \end{cases}, \tag{1}$$

where $\bar{n}=n_{imp}^2/4n^*$. Here the carrier concentration n on the graphene layer is used as $n=C_{ox}V_g$, where C_{ox} is the gate capacitance and V_g is the gate voltage. Figure 1(c) shows the calculated conductivity as a function of the gate voltage for impurity concentrations ranging from 2×10^{11} to 10×10^{11} cm^{-2}.

For a bias point, the carrier density changes along the channel. Knowing the gate voltage dependence of the conductivity, the carrier density is calculated as a function of position along the channel. We have considered a constant contact resistance R_s of 1.2 kΩ (Ref. 24) between the source/drain electrodes and the graphene layer. For a two-dimensional FET model, the drain current is written as[25]

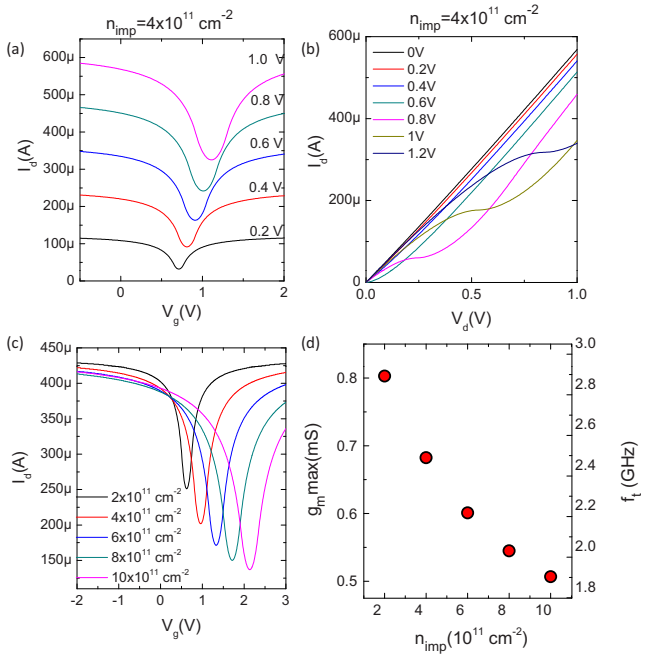

FIG. 2. (Color online) (a) The transfer curves for a graphene FET with a channel length of 1 μm and channel width of 1 μm. The gate dielectric used for the calculation is 50 nm HfO_2. A clear ambipolar behavior and current saturation because of contact resistance is seen on the transfer curves. (b) The output curves of the same device for the gate voltage range from 0 to 1.2 V. The curves in (a) and (b) are calculated for n=4 $\times10^{11}$ cm^{-2}. (c) The transfer curves for the device for different charged impurity concentrations at a drain voltage of 0.6 V. (d) Calculated maximum transconductance of the device as a function of charged impurity concentration.

$$I_d = \frac{W}{L_c}\int_0^{L_c} \sigma(x)E(x)dx = \frac{W}{L_c}\int_{V_s-R_sI_d}^{V_d-R_sI_d} \sigma(V)dV, \tag{2}$$

where $\sigma(x)$ is the conductivity and $E(x)$ is the electric field along the graphene layer. With a change of variable including the voltage drops at the contacts, the integral becomes a simple transcendental equation. Solving this transcendental equation using the conductivity values calculated by Eq. (1) provides the drain current for a given biasing condition. Figures 2(a) and 2(b) show transfer and output curves of a device with a channel length of 1 μm and channel width of 1 μm. In this calculation we have used a 50 nm HfO_2 as a gate dielectric with a dielectric constant of 16. For these calculation, the only empirical parameter that we used is impurity concentration on the dielectric and contact resistance between the electrodes and the graphene. This framework allows us to analyze the effect of the gate dielectric material on the device performance. Figure 2(c) shows the calculated transfer curves for different concentration of charge impurities on the substrate. The Dirac point shifts to the higher voltages and the on/off ratio increases with increasing charge impurity concentration. The on/off ratio of the devices increases from 1.7 to 3.0 as the impurity concentration increases. Dependence of on/off ratio on the impurity concentration can be understood from the decreasing in minimum conductivity of the graphene layer as the impurity concentration increases. This behavior provides a tradeoff between transconductance and output resistance for the high frequency performance.

High frequency performance limits can be understood by analyzing the cut-off frequency (f_t) of the device. Cut-off

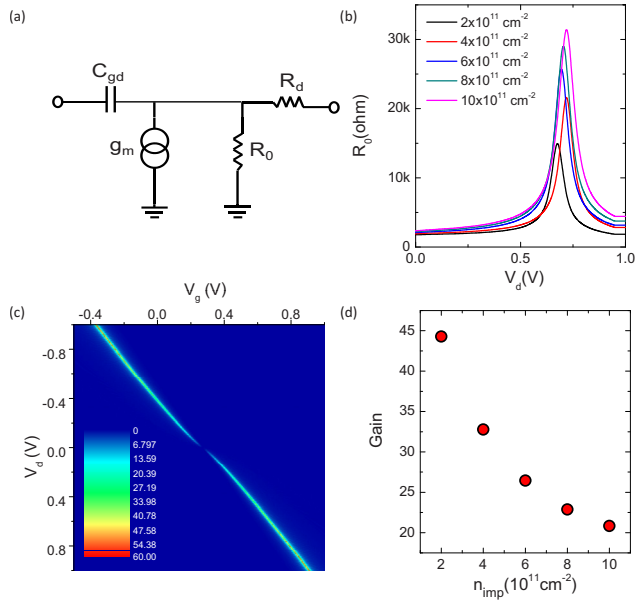

FIG. 3. (Color online) (a) The simplified small signal circuit model for the graphene FET. Here g_m is transconductance, R_0 is output resistance, R_d is drain resistance, and C_{gd} is the intrinsic gate-drain capacitance. (b) The output resistance calculated from the output curves for different impurity concentration ranging from the cleanest to the dirtiest sample. (c) Two-dimensional map of small signal power gain of the device. The x and y axis represents gate and drain voltages, respectively. (d) Maximum available gain of the device as a function of charged impurity concentration.

frequency is defined as the frequency where the current gain is 0 dB. After cut-off frequency the drain current due to the modulation of the channel conductivity is less than the gate leakage current. Gate capacitance and the small signal transconductance of a device determine the cut-off frequency as $f_t = g_m / 2\pi C_g$. Figure 2(d) shows the calculated maximum transconductance of the device and the associated cut-off frequency as function of charged impurity concentration. The parallel plate gate capacitance is used for the calculation. Cleanest samples with charged impurity levels of 2×10^{11} have f_t around 25 GHz for 1 μm channel length. The calculated cut-off frequency decays down to 18 GHz as we increase the charged impurity concentration.

A small signal circuit model for the graphene devices is presented to understand the intrinsic high frequency performance. A simplified small-signal equivalent circuit model of a graphene device is given in Fig. 3(a). C_{gd}, g_m, R_d, and R_0 represent gate-drain capacitance, transconductance, drain resistance and the output resistance of the device round a bias point, respectively. We have not used the source-gate capacitance because it will be much smaller than the drain-gate capacitance at the saturation regime.[16] Graphene FETs have very small on/off ratios owing to a large minimum conductivity at the Dirac Point. This minimum conductivity limits the output resistance of the device. The output resistance, defined as $R_0 = (\partial I_d / \partial V_d)^{-1}$, plays a critical role in the high frequency operation especially for the signal amplification. Figure 3(b) shows the output resistance as a function of the drain voltage. Large output resistance ($\sim$30 kΩ) can be achieved at a very narrow range of drain and gate voltages. The knowledge of output resistance and transconductance provides the power gain of the device. Power gain of a transistor used as an amplifier is another important parameter for high frequency operation. Power gain is defined as $G = g_m R_0$ where g_m is the transconductance, and R_0 is the output resistance. The highest available gain for a device with a given impurity concentration is given in Fig. 3(d). A gain of 45 can be achieved for the impurity concentration around 2×10^{11} cm^{-2}. The most striking point here is that even devices with a very poor on/off ratio can provide power gain at suitable biasing conditions. The results reveal that graphene transistors can be used for rf power amplifiers.

In this Letter we provide a simple yet quantitative framework to model the high frequency performance of graphene based field effect transistors. The model uses a self consistent charge transport mechanism based on a charge impurity scattering. The effect of contact resistance, minimum conductivity, and gate dielectric is studied. Basic device considerations for analog electronic applications such as output resistance and power gain are discussed. Although graphene has very unusual device performance, radio frequency analog electronics could be an immediate high-end application.

This work was supported by the Scientific and Technological Research Council of Turkey (TUBITAK) under Grant No. 109T259, and Marie Curie International Reintegration Grant (IRG) under Grant No 256458.

[1] K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, J. H. Ahn, P. Kim, J. Y. Choi, and B. H. Hong, Nature (London) **457**, 706 (2009).
[2] X. S. Li, W. W. Cai, J. H. An, S. Kim, J. Nah, D. X. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, Science **324**, 1312 (2009).
[3] A. Reina, X. T. Jia, J. Ho, D. Nezich, H. B. Son, V. Bulovic, M. S. Dresselhaus, and J. Kong, Nano Lett. **9**, 30 (2009).
[4] J. A. Rogers, Nat. Nanotechnol. **3**, 254 (2008).
[5] S. Unarunotai, Y. Murata, C. E. Chialvo, H. S. Kim, S. MacLaren, N. Mason, I. Petrov, and J. A. Rogers, Appl. Phys. Lett. **95**, 202101 (2009).
[6] J. W. Bai, X. Zhong, S. Jiang, Y. Huang, and X. F. Duan, Nat. Nanotechnol. **5**, 190 (2010).
[7] F. N. Xia, D. B. Farmer, Y. M. Lin, and P. Avouris, Nano Lett. **10**, 715 (2010).
[8] V. P. Verma, S. Das, I. Lahiri, and W. Choi, Appl. Phys. Lett. **96**, 203108 (2010).
[9] Y. Lee, S. Bae, H. Jang, S. Jang, S. E. Zhu, S. H. Sim, Y. I. Song, B. H. Hong, and J. H. Ahn, Nano Lett. **10**, 490 (2010).
[10] S. Bae, H. Kim, Y. Lee, X. F. Xu, J. S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. R. Kim, Y. I. Song, Y. J. Kim, K. S. Kim, B. Ozyilmaz, J. H. Ahn, B. H. Hong, and S. Iijima, Nat. Nanotechnol. **5**, 574 (2010).
[11] F. Schwierz, Nat. Nanotechnol. **5**, 487 (2010).
[12] F. N. Xia, T. Mueller, Y. M. Lin, A. Valdes-Garcia, and P. Avouris, Nat. Nanotechnol. **4**, 839 (2009).
[13] Y. M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H. Y. Chiu, A. Grill, and P. Avouris, Science **327**, 662 (2010).
[14] C. Kocabas, H. S. Kim, T. Banks, J. A. Rogers, A. A. Pesetski, J. E. Baumgardner, S. V. Krishnaswamy, and H. Zhang, Proc. Natl. Acad. Sci. U.S.A. **105**, 1405 (2008).
[15] C. Rutherglen, D. Jain, and P. Burke, Nat. Nanotechnol. **4**, 811 (2009).
[16] C. Kocabas, S. Dunham, Q. Cao, K. Cimino, X. N. Ho, H. S. Kim, D. Dawson, J. Payne, M. Stuenkel, H. Zhang, T. Banks, M. Feng, S. V. Rotkin, and J. A. Rogers, Nano Lett. **9**, 1937 (2009).
[17] S. J. Kang, C. Kocabas, T. Ozel, M. Shim, N. Pimparkar, M. A. Alam, S. V. Rotkin, and J. A. Rogers, Nat. Nanotechnol. **2**, 230 (2007).
[18] Y. M. Lin, K. A. Jenkins, A. Valdes-Garcia, J. P. Small, D. B. Farmer, and P. Avouris, Nano Lett. **9**, 422 (2009).
[19] F. Chen, J. L. Xia, and N. J. Tao, Nano Lett. **9**, 1621 (2009).
[20] F. Chen, J. L. Xia, D. K. Ferry, and N. J. Tao, Nano Lett. **9**, 2571 (2009).
[21] J. H. Chen, C. Jang, S. Adam, M. S. Fuhrer, E. D. Williams, and M. Ishigami, Nat. Phys. **4**, 377 (2008).
[22] S. Adam and S. Das Sarma, Solid State Commun. **146**, 356 (2008).
[23] S. Adam, E. H. Hwang, V. M. Galitski, and S. Das Sarma, Proc. Natl. Acad. Sci. U.S.A. **104**, 18392 (2007).
[24] S. Russo, M. F. Craciun, M. Yamamoto, A. F. Morpurgo, and S. Tarucha, Physica E (Amsterdam) **42**, 677 (2010).
[25] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, Nat. Nanotechnol. **3**, 654 (2008).