Materials Science in Semiconductor Processing 39 (2015) 400–407

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Capacitance–conductance–current–voltage characteristics of atomic layer deposited Au/Ti/Al_2O_3/*n*-GaAs MIS structures

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ARTICLE INFO

Available online 6 June 2015

ABSTRACT

We have studied the admittance and current–voltage characteristics of the Au/Ti/Al_2O_3/*n*-GaAs structure. The Al_2O_3 layer of about 5 nm was formed on the *n*-GaAs by atomic layer deposition. The barrier height (BH) and ideality factor values of 1.18 eV and 2.45 were obtained from the forward-bias ln *I* vs *V* plot at 300 K. The BH value of 1.18 eV is larger than the values reported for conventional Ti/*n*-GaAs or Au/Ti/*n*-GaAs diodes. The barrier modification is very important in metal semiconductor devices. The use of an increased barrier diode as the gate can provide an adequate barrier height for FET operation while the decreased barrier diodes also show promise as small signal zero-bias rectifiers and microwave. The experimental capacitance and conductance characteristics were corrected by taking into account the device series resistance R_s. It has been seen that the non-correction characteristics cause a serious error in the extraction of the interfacial properties. Furthermore, the device behaved more capacitive at the reverse bias voltage range rather than the forward bias voltage range because the phase angle in the reverse bias has remained unchanged as 90° independent of the measurement frequency.

1. Introduction

To achieve a large current drive in a MOSFET (metal-oxide-semiconductor field-effect transistor), a large interfacial layer capacitance is desirable. As the thickness of the gate oxide is reduced below a few nanometers, tunnel current can flow between gate and substrate. One method used to increase interfacial layer capacitance without generating excess gate current is to use materials other than SiO_2 as the dielectric gate. These materials have a high dielectric constant value, compared to SiO_2 (k=3.9). That is, the high dielectric constant-oxides such as TiO_2, Si_3N_4, Al_2O_3 and SnO_2 offer MOS gate dielectric electronic applications that are unattainable with SO_2-based devices [1–4]. Due to its influence on channel mobility, threshold voltage control and reliability of the MOSFET, the high-*k* oxide/silicon interface plays a crucial role in future gate stack development [1–5]. Many different methods are used to form the gate oxide layer in the semiconductor devices. Atomic layer deposition (ALD) is one of the thin film fabrication techniques. The ALD is an emerging ultra-thin deposition technology [2–6]. Ye et al. [2] have stated that the ALD is a surface controlled layer-by-layer process for the deposition of thin films with atomic layer accuracy.

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http://dx.doi.org/10.1016/j.mssp.2015.05.025
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Each atomic layer formed in the sequential process is a result of saturated surface controlled chemical reactions. They [6] have reported on a GaN metal-oxide-semiconductor high-electron-mobility-transistor (MOS-HEMT) using ALD Al_2O_3 as the gate dielectric. Compared to a conventional GaN HEMT of similar design, the MOS-HEMT exhibits several orders of magnitude lower gate leakage and several times higher breakdown voltage and channel current. The quality of the ALD Al_2O_3 is also much higher than those deposited by other methods, i.e., sputtering and electron-beam deposition, in terms of uniformity, defect density and stoichiometric ratio of the films [2–6].

We have prepared the MIS (metal/insulator/semiconductor) Au/Ti/Al_2O_3/*n*-GaAs/In. The Al_2O_3 metal oxide layer on the GaAs substrate was formed by an ALD method, and the film thickness of the Al_2O_3 layer was about 5 nm. As stated by Pan et al. [7], the complementary MOS devices require the gate oxide of about 1 nm to reduce the gate leakage current and maintain the gate capacitance. This is the reason why we take such a thickness [7]. The thickness of conventional SiO_2 less than 20 Å is inevitable to excessive leakage current due to the occurrence of direct tunneling. Therefore, silicon dioxide has to be substituted by a high dielectric constant material, which provides a physically thicker film for the same electrically equivalent oxide thickness [1–7]. The Au(50 nm)/Ti(10 nm) Schottky contacts have been fabricated on Al_2O_3/*n*-GaAs structure using magnetron DC sputter technique by us. Au thin films are more often used as a top layer to protect other metallic layers. Al_2O_3 is an attractive candidate for the high-κ material; it has a dielectric constant of 8.6 and a wide bandgap of about 6.6 eV. Titanium is commonly used as a standard gate metal in the fabrication of GaAs FET and MESFET since it has good adhesion and is stable against inter-diffusion and compound formation and has good electrical properties at room temperature and elevated temperatures [1–7].

We have studied the admittance and current–voltage (*I–V*) characteristics of the Au/Ti/Al_2O_3/*n*-GaAs structure with the Al_2O_3 layer about 5 nm. Fig. 1 shows the schematic model of the Au/Ti/Al_2O_3/*n*-GaAs structure. The interfacial layer at the metal–semiconductor interface can be also used for Schottky barrier modification [8–16].

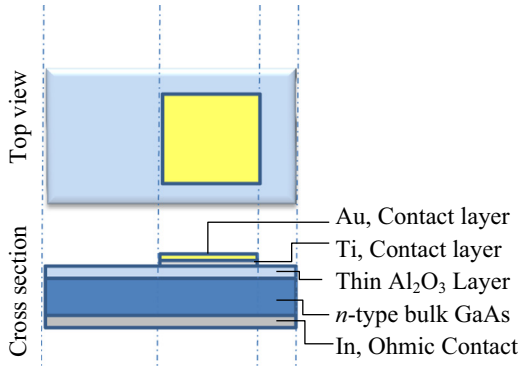

Fig. 1. Schematic model of the Au/Ti/Al_2O_3/*n*-GaAs structure.

The barrier modification using interfacial layer also is very important in Schottky diodes or metal semiconductor devices. Decreased barrier diodes also show promise as small signal zero-bias rectifiers and microwave mixers. In one microwave rectifier application, conventional diodes having larger barrier heights must be used with a dc offset voltage. Reduced barrier devices can be used in a preferable zero-bias mode. The increased barrier structures are useful for the gates of MESFETs [8]. The use of an increased barrier diode as the gate can provide an adequate barrier height for FET operation. As mentioned above, increased barrier devices are also useful in surface recombination studies by suppressing the thermionic emission (TE) current sufficiently such that $2kT$ recombination currents can be detected. Increased barrier diodes may also be useful as optical detectors, for example as solar cells and photodiodes, although there is a question as to electron reflection in the vicinity of the potential maximum. Furthermore, since increased barrier devices can be fabricated which range continuously from majority$\sim$ carrier dominated Schottky diodes to bipolar *pn* junctions, these structures should be useful in studies of minority-carrier lifetimes and carrier diffusion constants.

2. Experimental details

The Au/Ti/Al_2O_3/*n*-GaAs structures were fabricated using *n*-type single crystals GaAs wafer with (100) surface orientation, having thickness of 300 μm, 6.8×10^{15} cm^{-3} carrier concentration (N_D) and 1.2 Ω cm resistivity (given by the manufacturer). The pre-gate treatment on the sample prior to ALD was only performed by successively immersing in acetone, propanol for 2 min and de-ionized water to remove the organic and inorganic impurity. Then, it was rinsed in DI water of resistivity of 18 MΩ cm for an extended time at the end and dried under N_2 flow. After surface cleaning of *n*-GaAs, high purity (99.999%) indium with a thickness of about 2000 Å was coated for ohmic contact at a base pressure about 10^{-6} Torr. Low ohmic contact to *n*-GaAs was obtained by annealing at 385 °C for 3 min under dry nitrogen flow. The Al_2O_3 interface layer is formed by the ALD method. The Al_2O_3 thin film was coated using Savannah 100 thermal ALD reactor (Ultratech/Cambridge Nanotech Inc.) at a substrate temperature of 200 °C using trimethylaluminum (TMA) and water (H_2O) as aluminum and oxygen precursors, respectively. Exposure time of 0.015 s was used for both precursors while the purge time was adjusted to 10 s. The resulting Al_2O_3 film growth rate was about 1.05 Å per cycle. Standard photolithography technique was used for pattern fabrication on GaAs. Au(90 nm)/Ti(10 nm) Schottky contacts are made using the magnetron DC sputter technique. Finally the photoresist was removed by washing with DI water and then with N_2. All the electrical characterizations are carried out using Keithley 2400 current source and 6514 electrometer. The *I–V* and C–*V* and-*G–V* characteristics of the device were measured using a Keithley 487 Picoammeter/Voltage Source and a HP 4192A LF Impedance Analyzer at room temperature in dark.

3. Results and discussion

Fig. 1 shows the experimental capacitance–voltage (*C–V*) characteristics for the MIS Au/Ti/Al_2O_3/*n*-GaAs structure with Al_2O_3 interfacial layer thickness of about 5 nm. The measurement frequency and temperature were 100 kHz and 300 K, respectively. In the forward bias case for the Au/Ti/Al_2O_3/*n*-GaAs/In structure, indium (*n*-GaAs/In or ohmic side) was negatively biased and Au/Ti (rectifying side) was positively biased in reverse bias, vice versa. The shape of the *C–V* curve in Fig. 1 is an evidence of the presence of the interfacial layer at metal and *n*-type GaAs interface. That is, for a MIS diode with *n*-type semiconductor, the *C–V* curve has an accumulation region of electrons and therefore a high differential capacitance of semiconductor in series with the capacitance of the insulator at negative voltage at left side. As a result, the total capacitance is close to the capacitance of the insulator in the accumulation region [14–19]. As the negative voltage is reduced sufficiently toward the positive voltage, a depletion capacitance forms near the semiconductor surface [14–19]. As can be seen from Fig. 2, the hysteresis is observed in two sweep directions, one is from the positive voltage to the negative voltage and other is from the negative voltage to the positive voltage. The possible reason of this behavior is due to the presence of mobile charges in the interfacial layer [14–19]. The hysteresis width can be regarded as a measure of the electron and hole trapping in the interfacial layer. Therefore, we may say that the interface states between the interfacial layer and the GaAs substrate contain a net negative charge due to the presence of the acceptor-like interface states that cause the hysteresis width. The hysteresis width can be accompanied by an increase in the film resistivity. The series resistance value of 7.0 kΩ for the MIS structure may be an evidence for that [20,21].

The characteristics parameters of the ideal Schottky diodes are calculated using the TE Thermionic emission (TE) current expression. The *I–V* equation by the forward bias TE theory is given as follows [14,15,22]:

$$I = I_0\left[\exp\left(\frac{q(V-IR_s)}{nkT}\right)-1\right], \quad (1)$$

where I_0 is the saturation current

$$I_0 = AA^*T^2\exp\left(-\frac{q\Phi_{b0}}{kT}\right), \quad (2)$$

is the saturation current density, Φ_{b0} and n are the effective barrier height (BH) at zero bias and ideality factor calculated from the intercept and slope of the linear portion of the semi-log forward bias ln *I–V* characteristics, respectively, A^* is the effective Richardson constant of 8.16 A cm^{-2} K^{-2} for *n*-type GaAs, and A is the diode area. R_s is the series resistance of the neutral region of the semiconductor substrate between the depletion region and ohmic contact. (V–IR_s) and IR_s are the voltage drop across the depletion region and the series resistance, respectively. Fig. 3 shows the semi-log reverse and forward current–voltage curves of the Au/Ti/Al_2O_3/*n*-GaAs device with Al_2O_3 layer thickness of about 5 nm at 300 K and the figure in and inset: experimental current–voltage characteristics for the reference Au/Ti/*n*-GaAs Schottky barrier diode (SBD) without interfacial layer at 300 K temperature. The downward curvature region of the forward bias *I–V* characteristics in Fig. 2 results from the series resistance R_s of the neutral region of the semiconductor substrate. When Eq. (1) is fitted to the experimental *I–V* data of both SBD, without and with interfacial layer at 300 K temperature over whole forward bias, the series resistance value was found to be about 130 Ω for without interfacial layer and 7.0 kΩ for with interfacial layer. The large value of 7.0 kΩ is supplied from the contribution of the semiconductor substrate plus Al_2O_3 interfacial layer plus imperfect ohmic contact to the neutral region series resistance.

At high currents there is always a deviation of the ideality that has been clearly shown to depend on the

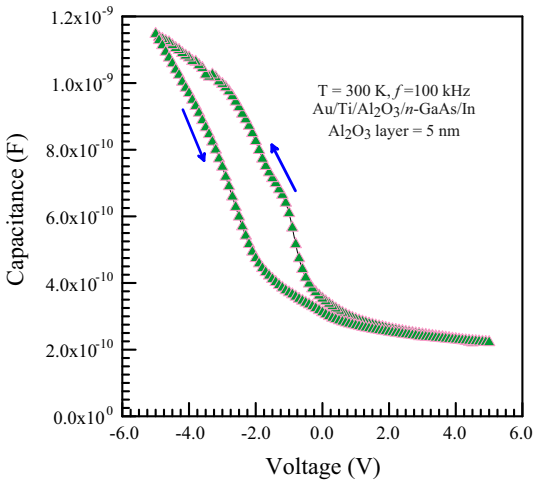

Fig. 2. Experimental forward and reverse bias capacitance–voltage characteristics for the MOS (metal/oxide layer/semiconductor) Au/Ti/Al_2O_3/*n*-GaAs structure with about 5 nm Al_2O_3 layer thickness at 100 kHz frequency and 300 K.

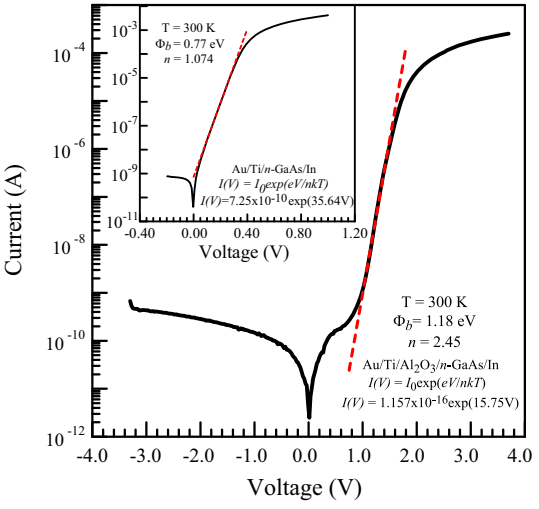

Fig. 3. Experimental current–voltage characteristics for Au/Ti/Al_2O_3/*n*-GaAs structure with about 5 nm Al_2O_3 interfacial layer thickness at 300 K and inset: experimental current–voltage characteristics for the reference Au/Ti/*n*-GaAs Schottky barrier diode without interfacial layer at 300 K.

series resistance, as one would expect. The lower the series resistance, the greater is the range over which ln *I*–*V* does infact yield a straight line. As the linear part of ln *I*–*V* plots is reduced, the accuracy of determination of barrier height and ideality factor is poor. As is widely known, the ohmic contact resistance must be very low to keep the series resistance of the device as small as possible. It has been well known that the SBDs (Schottky barrier diode) with and without interfacial layer are usually called the MIS and intimate SBDs, respectively, with the perfect or imperfect ohmic contact. The series resistance of an intimate MS contact must only come from the substrate bulk, that of a MIS SBD from the substrate bulk plus the interfacial layer. If the series resistance of the intimate MS contact is more than the substrate bulk, then it can be said that the ohmic contact resistance contributes to the series resistance of the device and such an ohmic contact is called imperfect ohmic contact.

The series resistance of the GaAs bulk substrate can be calculated from $R_B=(\rho L)/A$, where $\rho=0.77\ \Omega$-cm and $L=375\ \mu$m and $A=0.01\ \text{cm}^2$ are the resistivity and bulk thickness of the GaAs and the area of the Schottky contact respectively. A value of about 3 Ω for R_B is obtained; thus, it can be said that the contribution of the imperfect ohmic contact to the both diodes is about 127 Ω because the series resistance value of the SBD without interfacial layer was about 130 Ω.

For $q(V–IR)$ greater than $3kT$, the ideality factor is given by

$$n=\frac{q}{kT}\frac{dV}{d(\ln I)}. \tag{3}$$

The value of n indicates the deviation from ideal forward bias characteristics for Schottky diodes. The experimental values of the BH and ideality factor from the intercept and slope of the linear portion of the forward-bias ln I vs V plot have been calculated as 1.18 eV and 2.45 at 300 K, respectively, for with interfacial layer structure, 0.77 eV and 1.074 at 300 K, respectively, for without interfacial layer structure. The high value of n for the MIS structure can be attributed to effects of the bias voltage drop across the interfacial layer plus the native oxide layer (such as As_2O3 and Ga_2O3), and therefore, of the bias voltage dependence of the barrier height [22,23]. The surface of GaAs may be inevitably covered with such a thin native oxide film between 10 and 20 Å depending on the method of surface preparation during the fabrication of the device. Metal–semiconductor contacts formed under these conditions are not intimate contacts because an interfacial native oxide layer of atomic dimensions inevitably separates them. The surface of GaAs is known to be present with oxides of Ga and As which are not very stable [13–16]. Goksu et al. [23] used the GaAs semiconductor substrate with the same carrier concentration ($7.43\times10^{15}\ \text{cm}^{-3}$) and fabricated for Ti/*n*-GaAs diodes without the interfacial layer prepared by magnetron DC sputtering and obtained a BH value of 0.90 eV with an ideality factor 1.02 for this diode at 300 K. Di Dio et al. [24] have reported BH values from 0.79 to 0.83 eV for *I*–*V* characteristics of Au/Ti/*n*-GaAs diodes prepared by ion beam sputtering at different sputtering voltages and currents at 300 K. Ayyildiz et al. [25] have given a BH value of about 0.64 eV with an ideality factor of 1.08 from forward bias *I*–*V* characteristics (300 K) of Ti/*n*-GaAs diodes prepared by evaporation of Ti. The barrier height value of 1.18 eV we have found for the Au/Ti/Al_2O_3/*n*-GaAs structure is larger than the reported values. The reason for difference can be due to the presence of the Al_2O_3 layer at the Au/Ti and *n*-GaAs interface. Therefore, it can be said that the Al_2O_3 layer can be used to realize the barrier height modification in the Schottky diodes. As mentioned above, the barrier increase is useful for the gates of MESFETs and in surface recombination studies by suppressing the thermionic emission current. The use of an increased barrier diode as gate provides an adequate barrier height for FET operation and the fabrication of the devices, which range from the majority carrier dominated Schottky diodes to bipolar *p*-*n* junctions [8-13]. The deviations from linearity at low bias voltages in the forward *I*–*V* part are due to the shunt resistance or excess current [26–29].

The barrier height change in the contacts with the interfacial layer depends on the presence of the interface charges between the interfacial layer and the semiconductor substrate. The increase in positive or negative charge present in the interface states will affect the depletion layer of the semiconductor. In *n*-type semiconductor substrate, positively charged donor-like interfacial charges will reduce the barrier height because the positive space charges in the depletion region decrease while negatively charged acceptor-like interfacial charges will increase it because the positive space charges in the depletion region increase [22,30–32]. Therefore, we may say that the presence of negatively charged interface acceptors between the interfacial layer and the GaAs substrate in the MIS sample will increase the BH with respect to the reference sample [22,30–32].

Figs. 4 and 5 show the experimental forward and reverse bias *C*–*V* and conductance–voltage (*G*–*V*) characteristics of the device at different frequencies and 300 K.

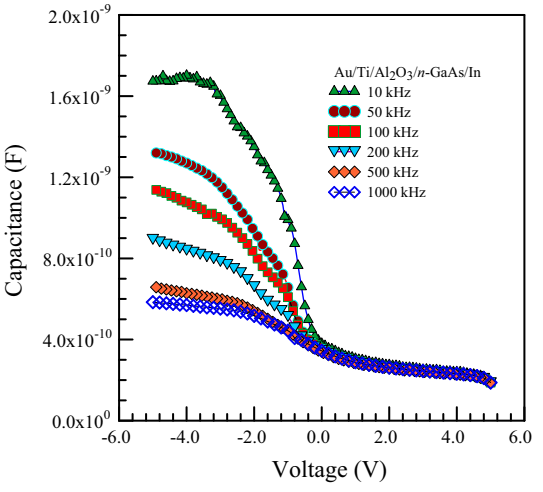

Fig. 4. Experimental forward and reverse bias capacitance–voltage characteristics for the Au/Ti/Al_2O_3/*n*-GaAs structure with about 5 nm Al_2O_3 interfacial layer thickness at different frequencies and 300 K.

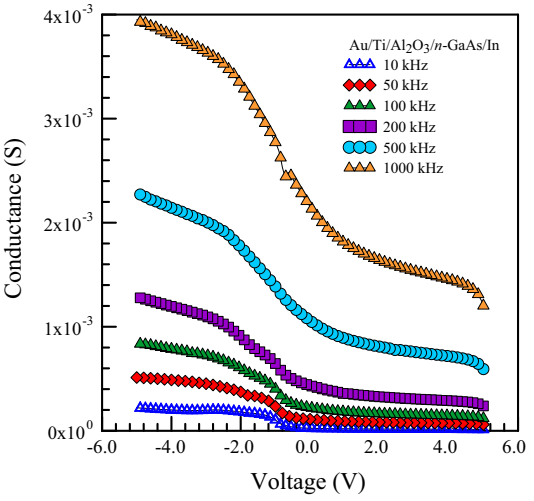

Fig. 5. Experimental forward and reverse bias conductance–voltage characteristics for the Au/Ti/Al_2O_3/*n*-GaAs structure with about 5 nm Al_2O_3 interfacial layer thickness at different frequencies and 300 K.

As can be seen, the capacitance value decreases (Fig. 4) while the conductance value (Fig. 5) increases with increasing frequency at a given bias voltage. The capacitance value decreases with increasing frequency because the charge at the interface states cannot follow the ac signal at sufficiently high frequencies [14–22,33–44]. As can be seen from Fig. 4, the capacitance curve saturates in the high forward bias voltage region. These saturation regions are known as the accumulation region giving the uncorrected capacitance of the interfacial layer (Al_2O_3) C_{ma} and thus its thickness. The experimental C_{ma} and G_{ma} values from the strong accumulation regions at each frequency in Figs. 4 and 5 are given in Table 1. The value of C_{ma} determined from the accumulation region in Fig. 5 decreases with increasing frequency. For example, we have obtained a value of about 1140 pF at 300 K and 100 kHz for the Au/Ti/Al_2O_3/*n*-GaAs structure. Pan et al. [7] have reported a value of about 500 pF at 300 K and 100 kHz for TiN/Nd_2O_3/*p*-Si/Al structure. They [7] have deposited the dielectric film with about 6.5 nm thickness onto Si substrate by rf magnetron sputtering from Nd target at a power of 175 W with a base pressure of 1×10^{-6} Torr. Lakshmi et al. [19] have reported a value of about 30 pF at 300 K and 1.0 MHz for Au/SiO_2/*n*-GaN structure, SiO_2 with 20 nm thickness. Saghrouni et al. [42] have obtained a value of about 300 pF at 300 K and 100 kHz for Co/Au/Dy_2O_3/*p*-GaAs structure. They [42] have deposited the dielectric Dy_2O_3 film with about 60 nm thickness onto *p*-GaAs substrate at 250 °C by electron beam with a growth rate of 0.2 Å/s under a pressure of 10^{-9} Torr. Likewise, Saghrouni et al. [43] have obtained a maximum value of about 2000 pF at 300 K and 1.0 MHz for Co/Au/Dy_2O3/*n*-GaAs structure. They [43] have deposited the dielectric Dy_2O_3 film with about 10 nm thickness onto *n*-GaAs substrate at 250 °C by electron beam with a growth rate of 0.2 Å/s under a pressure of 10^{-9} Torr. They stated [43] that the forward bias *C–V* curves change to negative values after a given forward bias voltage and that the material displays an inductive behavior and abnormal behavior. They [43] revealed that the values of *C* reach a maximum value and decrease rapidly with the increasing bias voltage in the forward bias region and take negative values. In ideal case, at high forward bias, the *C–V* curves should tend to saturate.

Fig. 6 shows the experimental reverse bias (A) capacitance–voltage and (B) C^{-2}–*V* characteristics for the Au/Ti/Al_2O_3/*n*-GaAs and the reference Au/Ti/*n*-GaAs (MS) structures at 100 kHz and 300 K respectively. As can be seen from the capacitance–voltage characteristics (A) of both samples, the capacitance value of the MIS structure is larger than that of the MS structure at each voltage. For

Table 1
The experimental parameters for the Au/Ti/Al_2O_3/*n*-GaAs structure with about 5 nm Al_2O_3 interfacial layer thickness at different frequencies and 300 K temperature, where C_{ma} and G_{ma} are the measured conductance and capacitance in the strong accumulation region, respectively, C_{0x} is the interfacial layer capacitance obtained using C_{ma} and G_{ma} in Eq. (4).

f (kHz)	C_{ma} (F)	G_{ma} (S)	$R(\Omega)$	C_{0x} (F)
10	1.68×10^{-9}	2.22×10^{-4}	3.67×10^{3}	1.42×10^{-9}
50	1.32×10^{-9}	5.12×10^{-4}	1.88×10^{3}	1.33×10^{-9}
100	1.14×10^{-9}	8.41×10^{-4}	680.00	2.07×10^{-9}
200	8.94×10^{-10}	1.29×10^{-3}	440.84	1.68×10^{-9}
500	6.60×10^{-10}	2.28×10^{-3}	240.10	1.46×10^{-9}
1000	5.84×10^{-10}	3.95×10^{-3}	135.60	1.26×10^{-9}

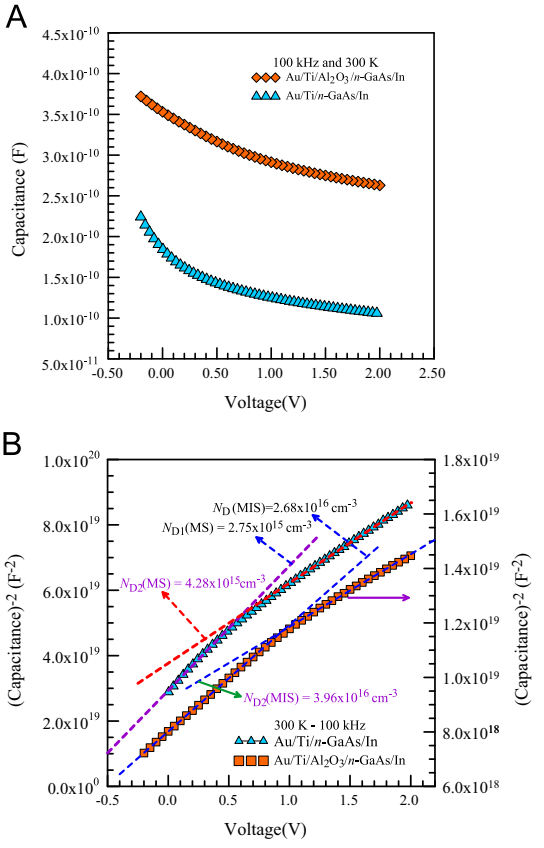

Fig. 6. Experimental reverse bias (A) capacitance–voltage and (B) C^{-2}–*V* characteristics for the Au/Ti/Al_2O_3/*n*-GaAs and the reference Au/Ti/*n*-GaAs structures at 100 kHz and 300 K.

example, the MIS structure has a capacitance value of 390 pF at 1.0 V while the MS structure has a capacitance value of 130 pF at 1.0 V. That is, the capacitance value of the MIS structure is three times larger than that of the MS structure. As indicated above, the positive space charges in the depletion region in the MIS structure are increased due to the presence of negatively charged interface acceptors between the Al_2O_3 interfacial layer and the GaAs substrate. Furthermore, the C^{-2}–V characteristics for the both structures have two slopes. One of the slopes is at low voltages, the other at high voltages. As can be seen from the values given in the figure, the carrier concentration found for the MIS structure is nearly 10 times larger than that of the MS structure due to the presence of the Al_2O_3 interfacial layer.

The series resistance can cause a serious error in the extraction of the interfacial properties. To avoid this error, a correction should be applied to the measured admittance before the desired information is extracted [14–19,33–43]. The series resistance R_s and the interfacial layer capacitance C_{0x} for the MOS structure can be calculated using the following equations [16]:

$$R_s = \left[\frac{G_{ma}}{(wC_{ma})^2 + G_{ma}^2}\right], \tag{4}$$

$$C_{ma} = \frac{C_{0x}}{1 + (wR_sC_{0x})^2}, \tag{5}$$

$$C_{0x} = C_{ma}\left[1 + \frac{C_{ma}^2}{(wC_{ma})^2}\right], \tag{6}$$

where $w = 2\pi f$ is the angular frequency of the ac signal and f is the frequency in Hz or s^{-1}. Eq. (6) was obtained from Eqs. (4) and (5). The C_{0x} and R_s values from Eqs. (4) and (6) for the accumulation region at each frequency are given in Table 1. Thus, the capacitance of the interfacial layer per area unit in a MIS diode is given by

$$C_{0x} = \frac{\varepsilon_{in}\varepsilon_0 A}{d}, \tag{7}$$

where ε_{in} and d are the permittivity of interfacial layer and its thickness, respectively, ε_0 is the permittivity of free space and A is the area of diode. A corrected value of 7.77 nm for the thickness of the interfacial layer Al_2O_3 was found using C_{0x} value at 10 kHz as given in Eq. (7). As can be known, the Al_2O_3 layer thickness formed on the GaAs wafer by the ALD method is about 5.0 nm. The higher-than-expected final thickness of 7.7 nm might be due to the native oxide layer grown on the GaAs substrate, within the limits of experimental error. Although the sample will stay for about 20 min within the ALD reactor at 200 °C; this most probably will cause a formation of a native oxide layer on the GaAs surface. As mentioned above, the decrease in the capacitance value with increasing frequency at a given bias voltage in the plots can be attributed to the decrease of the dielectric constant value of the interfacial layer Al_2O_3 with increasing frequency. As can be seen in Table 1, the series resistance value at each frequency is large enough to affect the capacitance. Therefore, the series resistance completely masks interface trap loss, and especially the equivalent parallel conductance is much more sensitive to the series resistance than capacitance. Thus, it can be said that the correction by taking account the series resistance is particularly important in conductance measurements [14–19,34–43].

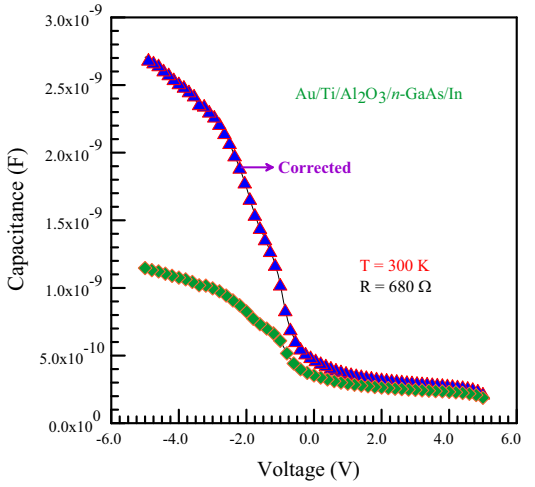

Fig. 7. Corrected and non-corrected experimental forward and reverse bias capacitance–voltage characteristics for the Au/Ti/Al_2O_3/n-GaAs structure with about 5 nm Al_2O_3 interfacial layer thickness at 100 kHz frequency and 300 K.

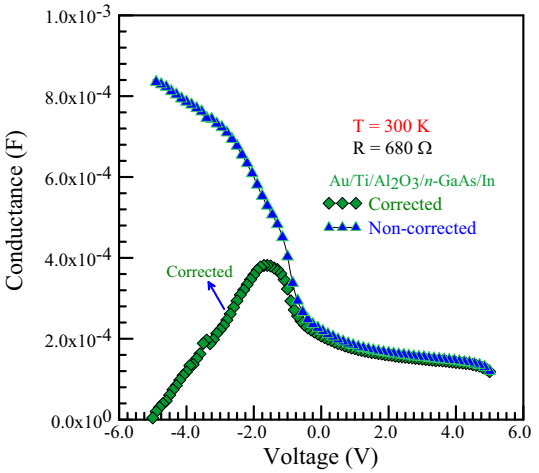

Fig. 8. Corrected and non-corrected experimental forward and reverse bias conductance–voltage characteristics for the Au/Ti/Al_2O_3/n-GaAs structure with about 5 nm Al_2O_3 interfacial layer thickness at 100 kHz frequency and 300 K.

For the MOS devices, corrected capacitance and equivalent parallel conductance at a given frequency can be written as follows [16]:

$$C_c = \frac{\left[G_m^2 + (wC_m)^2\right]C_m}{(wC_m)^2 + a^2}, \tag{8}$$

$$G_c = \frac{\left[G_m^2 + (wC_m)^2\right]C_m}{(wC_m)^2 + a^2} = \frac{(wC_cR_s)^2}{1 + (wC_cR_s)^2}, \tag{9}$$

where $a = G_m - \left[G_m^2 + (wC_m)^2\right]R_s$ and C_m and G_m are the capacitance and the equivalent parallel conductance

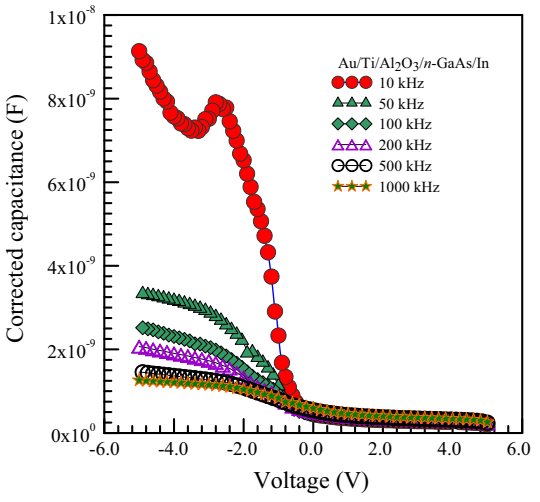

Fig. 9. Corrected experimental forward and reverse bias capacitance–voltage characteristics for the Au/Ti/Al_2O_3/*n*-GaAs structure with about 5 nm Al_2O_3 interfacial layer thickness at different frequencies and 300 K.

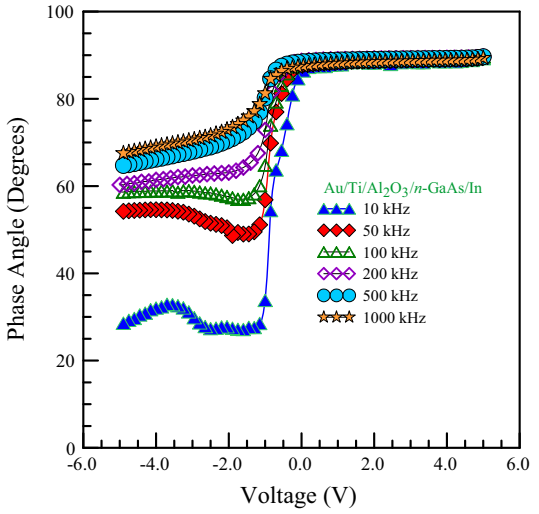

Fig. 11. Experimental forward and reverse bias phase angle–voltage characteristics for the Au/Ti/Al_2O_3/*n*-GaAs structure with about 5 nm Al_2O_3 interfacial layer thickness at different frequencies and 300 K.

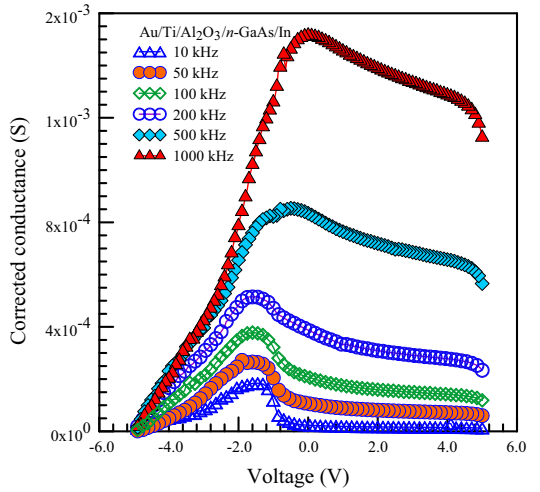

Fig. 10. Corrected experimental forward and reverse bias conductance–voltage characteristics for the Au/Ti/Al_2O_3/*n*-GaAs structure with about 5 nm Al_2O_3 interfacial layer thickness at different frequencies and 300 K.

measured across the terminals of the MOS capacitor at each frequency, that is, C_m and G_m values come from the experimental *C*–*V* and *G*–*V* curves in Figs. 4 and 5 respectively. Figs. 7 and 8 show the corrected and non-corrected experimental forward and reverse bias *C*–*V* and *G*–*V* characteristics for the device at 100 kHz frequency and 300 K temperature, as an example, respectively. The R_s value from the accumulation region using Eq. (4) at each frequency is used in these calculations. The absence of a peak in the non-corrected *G*–*V* curves means that the series resistance produced the dominant loss, completely masking the interface trap loss. The series resistance effect is clearly apparent in Figs. 7 and 8, and the greatest error in the capacitance occurs in accumulation and a portion of the depletion region [16,34–43]. As can be seen, it is not possible to neglect series resistance in every case. Therefore, the series resistance must be measured and applied as a correction to the measured admittance [16,34–43].

Figs. 9 and 10 show the corrected experimental forward and reverse bias *C*–*V* and *G*–*V* characteristics for the MOS structure at different frequencies and 300 K temperature, respectively. As mentioned above, the series resistance effect on the device characteristics is clearly apparent when the corrected *C*–*V* and *G*–*V* characteristics are compared to the uncorrected ones at each frequency. For example, the corrected capacitance value of 1.50×10^{-9} F is 2.27 times larger than the uncorrected capacitance value of 6.60×10^{-10} F at 500 kHz, and the corrected conductance value of 2.10×10^{-4} S is about 10 times lower than the uncorrected conductance value of 2.28×10^{-3} S at 500 kHz. When considering the corrected conductance–voltage curves in Fig. 11, it is seen that the observed conductance peak due to the correction shifts from the negative voltage to positive voltage and that the value of the conductance at the peak tends to increase with increasing frequency.

Fig. 11 shows the experimental forward and reverse bias phase angle–voltage characteristics for the MOS structure at different frequencies and 300 K. When considering Fig. 11, the device behaves more capacitive at the reverse bias voltage range rather than the forward bias voltage range because the phase angle has remained almost unchanged as 90° in the reverse bias range of 0.0–5.0 V at all frequencies [44,45]. In the forward bias part from −5.0 to 0.0 V, the phase angle increased with increasing frequency at a given voltage, that is, it has taken the values of 30° at 10 kHz and about 70° at 1000 kHz. Therefore, because of the phase angle characteristics, it can be said that the MOS structure behaves more capacitive at the reverse bias regime rather than the forward bias regime as independent of the measurement frequency. Furthermore, it can be concluded that the device becomes

too conductive with decreasing frequency in the forward bias regime [44,45].

4. Conclusion

In conclusion, it has been seen that the BH value of 1.18 eV obtained for the Ti/Al_2O_3/*n*-GaAs the interfacial layer is larger than those of the conventional Ti/*n*-GaAs diodes reported in the literature. It has been well-known that an increased barrier-diode as the gate can provide an adequate barrier height for FET operation. Therefore, it has been concluded that the barrier modification is very important in metal semiconductor devices. A correction by considering the device series resistance was applied to the experimental *C* and *G* characteristics before the desired information is extracted from the measured admittance because the series resistance effect is the greatest error in the *C* and G data which occurs in accumulation and a portion of the depletion region. After the correction, a large difference between the corrected and non-corrected admittance data was observed. The appearance of the peaks in *G*–*V* curves after correction means that the series resistance must be applied as a correction to the measured admittance. The device behaves more capacitive at the reverse bias voltage range rather than the forward bias voltage range because the phase angle has remained almost unchanged as 90° at all frequencies.

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