Journal of Physics and Chemistry of Solids 170 (2022) 110976

Contents lists available at ScienceDirect

Journal of Physics and Chemistry of Solids

journal homepage: www.elsevier.com/locate/jpcs

Plasma-enhanced atomic layer deposition of amorphous Ga_2O_3 gate dielectrics

Yosef Badali [a,*], Engin Arslan [b,c], Turkan Gamze Ulusoy Ghobadi [d], Suleyman Ozcelik [e], Ekmel Ozbay [c,f,g]

[a] Department of Computer Engineering, Istanbul Ticaret University, 34840, Istanbul, Turkey
[b] Department of Electrical and Electronics Engineering, Antalya Bilim University, 07190, Antalya, Turkey
[c] Nanotechnology Research Center, Bilkent University, 06800, Ankara, Turkey
[d] National Nanotechnology Research Center, Bilkent University, 06800, Ankara, Turkey
[e] Department of Physics, Faculty of Sciences, Gazi University, Ankara, Turkey
[f] Department of Electrical and Electronics Engineering, Bilkent University, 06800, Ankara, Turkey
[g] Department of Physics, Bilkent University, 06800, Ankara, Turkey

ARTICLE INFO

Keywords:
Atomic layer deposition
Amorphous Ga_2O_3
Dielectric properties
Interface traps

ABSTRACT

Amorphous gallium oxide (Ga_2O_3) thin films were investigated as gate dielectrics for electronic device applications using plasma-enhanced atomic layer deposition. The structural and morphological properties as well as the electrical and dielectric behaviors of Ga_2O_3 thin films were explored. The surface morphology of the amorphous Ga_2O_3 thin film was highly smooth with root mean square of 0.55 nm and low defect density, which were visible to atomic force microscopy. The grazing incidence X-ray diffraction pattern showed no discernible peak, indicating that the film was amorphous. The X-ray photoelectron spectroscopy depth-profiling analysis showed that the Ga/O ratio was 0.76, slightly more than the optimum 2/3 ratio (0.67). The temperature-dependent current–voltage characteristics of the Au/Ni/Ga_2O_3/p-Si structure revealed that ideality factor and barrier height values decreased and increased with increasing temperature, respectively, demonstrating their high temperature dependency. Regardless of the applied frequency, Ga_2O_3 thin films exhibited a good dielectric constant of about ~9 at zero bias voltage. The comprehensive capacitance–voltage analysis showed low trap densities of about 10^{12} eV^{-1} cm^{-2} at the Ga_2O_3–p-Si interface.

1. Introduction

Gate dielectrics have been researched for passivating surfaces, suppressing leakage current while improving breakdown strengths, and providing effective electrostatic control of the gate. Different high-k materials have been investigated as possible dielectric layers, including Al_2O_3, Y_2O_3, HfO_2, and TiO_2 [1–4]. These high-k materials, however, often require post-deposition annealing and may crystallize or react with the underlying Si substrate which is undesirable. Crystalline gallium oxide (β-Ga_2O_3) is a transparent conducting oxide with an ultra-wide bandgap of 4.9 eV, whereas amorphous Ga_2O_3 is only an electrical insulator because the combination of an ultra-wide bandgap and an amorphous structure makes electronic conduction extremely difficult. Amorphous Ga_2O_3 with the characteristics of wide bandgap, high dielectric constant, and perfect thermal stability causes a reduction of the direct tunneling leakage current [5]. Moreover, since the crystallization process in this material takes place at high temperatures, its passivation property is not lost during the deposition process at low temperatures. It has also been reported that the doped and undoped Ga_2O_3 amorphous structure significantly reduces the interfacial density states and leakage current when used as a gate dielectric in electronic devices [6–9]. These characteristics make Ga_2O_3 excellent as a dielectric material in next generation applications. The structure and electrical behavior of Ga_2O_3 thin films should, therefore, be routinely studied as dielectric layers, and their applicability to the manufacturing process should be defined for semiconductor devices. However, the dielectric properties of Ga_2O_3 structures have not yet been studied in detail.

So far, various growth processes, such as metal–organic chemical vapor deposition, molecular beam epitaxy, chemical bath deposition, and atomic layer deposition (ALD), have been used to create Ga_2O_3 thin

* Corresponding author.
E-mail address: ybedeli@ticaret.edu.tr (Y. Badali).

https://doi.org/10.1016/j.jpcs.2022.110976
Received 10 November 2021; Received in revised form 23 August 2022; Accepted 24 August 2022
Available online 30 August 2022

films [10–12]. Of these, ALD stands out because of its low temperature deposition and three-dimensional conformal deposition resulting from a self-limiting surface reaction and the superior regulation of thickness. Use of ALD can also ensure greater step coverage over substrates with large aspect ratios, which is necessary for a reliable dielectric gate [12]. Plasma-enhanced ALD (PEALD) technology has the advantage of extending the ALD process window toward lower temperatures by improving the chemical reaction [13]. For metal/oxide/semiconductor (MOS) applications, the use of Ga_2O_3 grown with PEALD could be the right option for a dielectric gate, since non-annealed Ga_2O_3 obtained by this method is an amorphous material with a high-k value (>9) and a comparatively wide bandgap (~4.8 eV) [14]. The PEALD-grown Ga_2O_3 dielectric layers also improve the crystallization temperature, decrease the interfacial oxide layer growth at the substrate–dielectric interface, and provide good interfacial dependability with the substrate [14].

It is critical to thoroughly investigate the charge-transport properties of amorphous Ga_2O_3-based MOS devices to effectively realize high-quality devices. In recent years, there have been many endeavors to manufacture Schottky structures with a Ga_2O_3 interface layer and to investigate their electrical characteristics at ambient temperature [15–17]. Unfortunately, the current–voltage (*I–V*) characteristics at ambient temperature do not give comprehensive information on charge-transport processes or the Schottky barrier interface's nature; however, investigations of temperature-dependent *I–V* behaviors are useful in this regard [18]. Understanding the dielectric properties of Ga_2O_3 interfaces is crucial for creating functional MOS devices. Thin films of Ga_2O_3 have been investigated as promising dielectric material for a variety of device applications, including deep-ultraviolet transparent films, dielectric coatings for solar cells, dielectric gates for MOS devices, and high-temperature sensors, due to their wide bandgap and good chemical and thermal stability [19]. Nevertheless, there are few detailed reports on the dielectric properties of amorphous Ga_2O_3 [20, 21].

In the present paper, we deposit Ga_2O_3 thin films on p-Si substrate to fabricate the MOS structure, and we explore the surface morphology and composition as well as the electrical and dielectric properties. The charge-transport mechanisms of this structure are studied using temperature-dependent *I–V* characteristics for 80–300 K. In addition, the dielectric behavior of the fabricated MOS structure is explored using frequency-dependent capacitance–voltage (*C–V*) and conductance–voltage ($G/\omega-V$) experiments. To better understand the characteristics of the Ga_2O_3–p-Si interfaces, the interface trap density (D_{it}) is estimated using admittance spectroscopy at ambient temperature.

2. Device structure and fabrication process

Deposition of the amorphous Ga_2O_3 thin film was implemented by PEALD system (Okyay ALD) using TEG ($(C_2H_5)_3Ga$) and O_2 plasma as precursors on 6 mm × 6 mm dimensional p-Si substrates. The growth process was begun by setting the reactor temperature and vacuum line temperature as 240 and 200 °C, respectively. An radio-frequency coil with an alternate radio-frequency power of 250 W was used to create the remote O_2 plasma. There were four stages in each ALD cycle: (1) TEG pulse, (2) Ar purge, (3) O_2 plasma, and (4) Ar purges. The films were deposited at a base pressure of $\sim 5 \times 10^{-4}$ bar and 250 °C. As a result of these stages, nominally 30-nm thick Ga_2O_3 film was grown on p-Si substrate verified using a spectroscopic ellipsometer (Jobin Yvon-Horiba).

Prior to the growth process, a 300-nm aluminum (Al) metal contact was put on the back side of the p-Si substrate. In order to form the ohmic contact, samples were annealed at 480 °C for 10 min in an N_2 atmosphere with rapid thermal annealing equipment. After the growth process, 1-mm diameter circular dot Schottky contact formation was carried out on the Ga_2O_3 thin film surface, using 100- and 50-nm thick nickel (Ni) and gold (Au), respectively.

3. Results and discussion

The grazing incidence X-ray diffraction (GIXRD) must be characterized to prove that the Ga_2O_3 thin film is amorphous. The GIXRD results of the Ga_2O_3 thin film show no discernible peak, indicating that the film is amorphous (Fig. 1a). The surface morphology of the amorphous Ga_2O_3 thin film grown on p-Si substrate, investigated using atomic force microscopy (AFM) imaging over a 3 μm × 3 μm scan size to demonstrate its surface quality, shows that the amorphous Ga_2O_3 has a crack-free, mirror-like surface form, and a smooth surface morphology with low roughness (root mean square = 0.55 nm) and low defect density (Fig. 1b).

X-ray photoelectron spectroscopy (XPS, Thermo Fisher Scientific, Al K-radiation, h = 1486.6 eV) in survey mode utilizing the flood gun for surface charge neutralization with 30 eV pass energy and 0.1 eV step size is used to investigate the surface elemental composition and binding energy (BE) values. Keeping the aliphatic C1s component at 284.8 ± 0.1 eV and adjusting other peaks in the spectra correspondingly is used to calibrate the BE scale. Depth-profiling is by using XPS with Ar^+ ions with 1000 eV energy. The samples' depth profiles are created in 14 cycles with a cycle duration of 20 s each.

The O1s and Ga3d spectra of the sample in both bulk and surface areas are shown in Fig. 2a–d. The O1s spectra in the surface is deconvoluted into two peaks: the sharp peak corresponding to low energy centered at 530.5 eV and a weak one corresponding to high energy centered at 532.4 eV. The peak at 530.5 eV is associated with Ga–O bond species. The peak at 532.4 eV is attributed to Ga–hydroxide bonds, such as OH^- or H_2O on the film surface. However, in the bulk medium, the O1s has a single peak response, showing successful growth of the Ga_2O_3 layer. In addition, emergence of the highly intense peaks at 20.25 eV (Fig. 2b and d) confirms the presence of Ga–O bonds, i.e. the creation of a Ga_2O_3 thin film. The O2s core level is a faint peak at higher (23.50 eV) BE [22]. Moreover, Ga3d orbitals have similar spectra for both surface and bulk regions. For a better qualitative comparison, the depth profile is extracted for the sample. The Ga:O ratio is calculated using data from the Ga3d and O1s core levels, as well as carbon concentrations (C1s data). The calculated Ga/O ratio is 0.76 (Fig. 2e), which is slightly more than the ideal ratio of 2/3 (0.67). This deviation from the ideal ratio indicates the presence of both Ga interstitial and O vacancies [22]. Moreover, the carbon contamination is only present in the surface and near surface regions. Therefore, the XPS depth-profiling analysis clearly shows the successful growth of the Ga_2O_3 layer. It should be mentioned that the purge time during the ALD growth cycle should be optimized to avoid introduction of carbon residues in grown metal oxide.

Fig. 3a shows the semilogarithmic *I–V* measurements of the Au/Ni/Ga_2O_3/p-Si structure recorded at 80–320 K in 20 K increments. The structure shows an exponential increase in forwarding bias current with a modest change in leakage current on the applied reverse bias, regardless of temperature, which is a characteristic property of a rectifying interface. The leakage current density at −2 V reverse bias changes from 2.4×10^{-6} to 1.7×10^{-3} A cm^{-2}, when temperature increases from 80 to 320 K (inset, Fig. 3a). These relatively remarkable leakage currents can be attributed to native oxides between the Ga_2O_3–p-Si interface and to the presence of both Ga interstitial and O vacancies. The slope and y-axis intercept of the ln(*I*)–*V* plots are used to determine the ideality factor (n) and barrier height (Φ_{b0}) for each temperature, with respect to thermionic emission theory [23,24]. When the temperature increases from 80 to 320 K, n and Φ_{b0} values change from 11.4 to 2.2 and 0.28–0.74 eV, respectively (Fig. 3b). That is, with increasing temperature, the n and Φ_{b0} values decrease and increase, respectively, demonstrating their high temperature dependency. However, the manufactured Au/Ni/Ga_2O_3 structure has a relatively high Φ_{b0} and low leakage current at 300 K, indicating a good-quality Ni Schottky contact created on the Ga_2O_3 in the current configuration. It also shows that the Ga_2O_3 layer has a good amorphous structure and exhibits an effective passivation feature. Barrier inhomogeneities at the Ni/Ga_2O_3 boundary

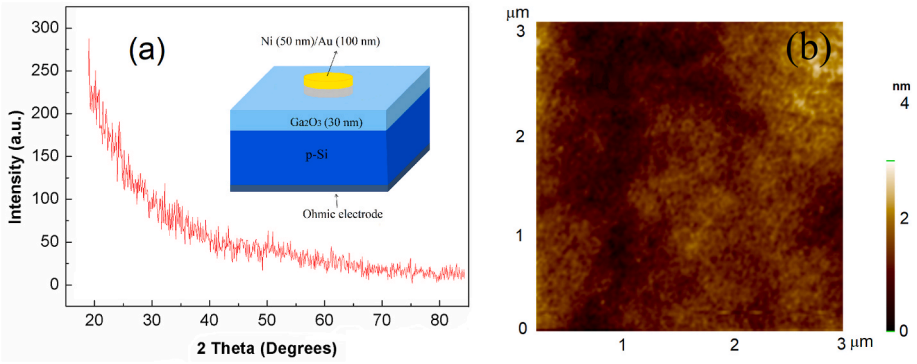

Fig. 1. (a) Grazing incidence X-ray diffraction (GIXRD) patterns, inset is a schematic of Au/Ni/Ga_2O_3/p-Si structure and (b) AFM image (3 μm × 3 μm scans) of the amorphous Ga_2O_3 layer deposited on p-Si substrate.

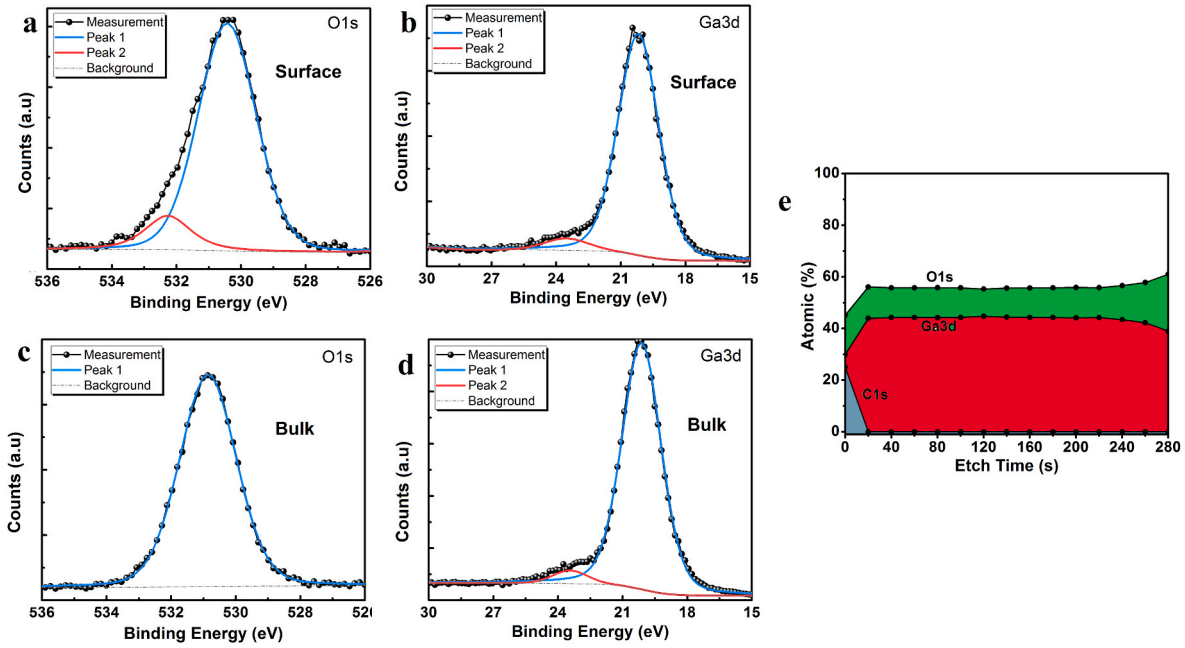

Fig. 2. XPS spectra of (a) O1s and (b) Ga3d for the Ga_2O_3 film surface, and (c) O1s and (d) Ga3d for the Ga_2O_3 thin film bulk. (e) Atomic percentage of elements Ga, O, and C in the ~30-nm thick amorphous Ga_2O_3 thin film obtained via XPS depth profiles. Total etching time of 280 s.

might explain the temperature-dependent characteristics of n and Φ_{b0}. The thermionic emission model considers the metal–semiconductor interface, which is atomically flat and geometrically homogeneous. The Schottky barriers of a variety of metal–semiconductor complexes, however, are rarely homogenous. A multitude of physical factors can create barrier inhomogeneity. These include poor interface quality, non-stoichiometries of the diffusion region, non-uniformity of the interlayer charge density, non-uniformity of the interface layer thickness, and doping atom distribution pattern. A local non-uniform Schottky barrier consists of substantially low and high Φ_{b0} regions of nanoscale size, which are expected to be dispersed according to a Gaussian distribution. Because the current predominantly passes through the patches with a low Φ_{b0} at lower temperatures, the patches with a high n dominate the current. However, at high temperatures, the current tends to pass through patches with a high Φ_{b0}, resulting in decreased n and increased Φ_{b0} [25,26].

An explanatory potential fluctuation model based on barrier height inhomogeneity with patchy contacts at the metal–semiconductor interface can clarify the abnormalities observed in Φ_{b0} and n. For contacts with patches with lateral dimensions less than the depletion width, the thermionic emission mechanism might still be efficacious [18]. As a result of the interface barrier being non-homogeneous, the barrier is not fixed, but instead complies with Gaussian distribution with different mean barrier height ($\overline{\Phi}_{b0}$) and standard deviation (σ_0) values. As a result, the dependency of Φ_{b0} on temperature may be deduced in terms of non-uniform Schottky contact using a Gaussian distribution of the barrier height with $\overline{\Phi}_{b0}$ and σ_0, with apparent barrier height (Φ_{ap}) and ideality factor (n_{ap}) provided as follows [27–30]:

$$\varphi_{ap} = \overline{\Phi}\mathrm{b0} - \frac{q\sigma_s^2}{2kT} \tag{1}$$

$$\frac{1}{n_{ap}(T)} - 1 = -\rho_2 + \frac{q\rho_3}{2kT} \tag{2}$$

where ρ_2 and ρ_3 are temperature-dependent voltage coefficients that characterize the voltage deformation of the Schottky barrier height distributions. Plots of Φ_{ap} and $1/n_{ap} - 1$ vs $q/2$ kT (Fig. 4) are derived using equations (1) and (2). In the 80–200 and 220–320 K temperature ranges, the Φ_{ap} and $1/n_{ap} - 1$ vs $q/2$ kT plots clearly reveal two linear regimes, showing a double Gaussian distribution of barrier heights. In the plot of Φ_{ap} vs $q/2$ kT, the linear fit of the data's y-axis intercept and slope provide $\overline{\Phi}_{b0}$ and σ_0, with values of 0.64 eV and 0.082 for 80–200 K,

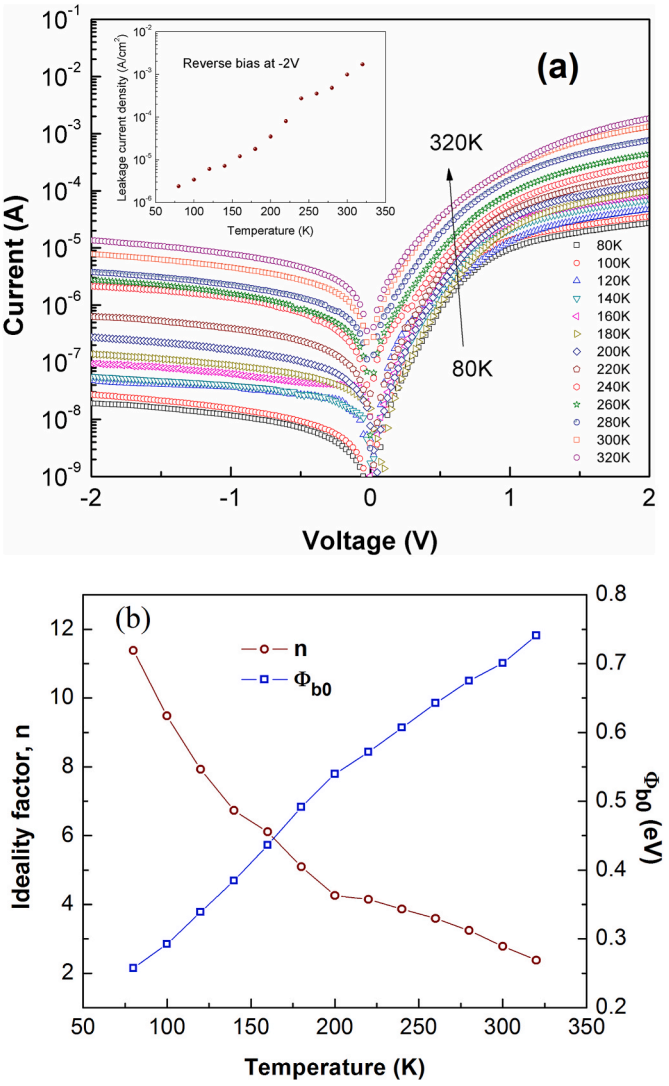

Fig. 3. (a) The temperature-dependent semi-log *I–V* characteristics in an experimental setting, inset is leakage current density vs temperature of the Au/Ni/Ga_2O_3/p-Si structure. (b) The Φ_{b0} and n vs temperature plots determined for Au/Ni/Ga_2O_3/p-Si structure.

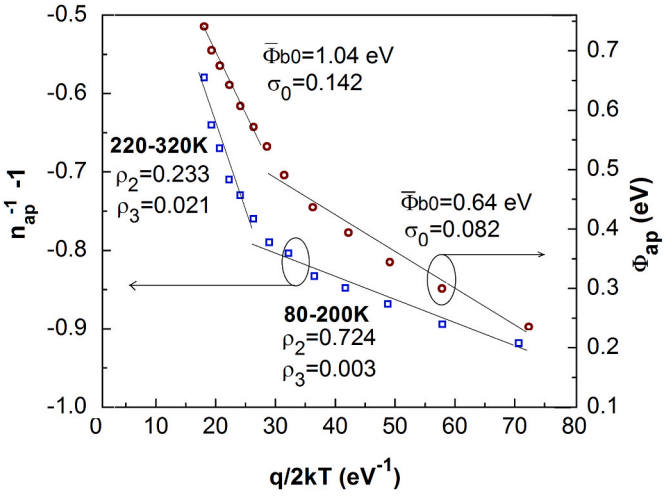

Fig. 4. The Φ_{ap} and $1/n_{ap} - 1$ vs $q/2$ kT plots of Au/Ni/Ga_2O_3/p-Si structure.

respectively, and correspondingly 1.04 eV and 0.142 for 220–320 K. The σ_0 value denotes the degree of barrier homogeneity such that smaller σ_0 indicates a more homogenous Schottky barrier created in the interface. The σ_0 values for the 80–200 and 220–320 K temperature ranges are not small enough to be insignificant compared to $\overline{\Phi}_{b0}$, suggesting the presence of non-homogeneous barrier height. Two linear regions are visible on the plot of $1/n_{ap} - 1$ vs $q/2$ kT, indicating the occurrence of double barrier height distribution. The y-axis intercept and slope of the linear fitted line of $1/n_{ap} - 1$ vs $q/2$ kT plot are ρ_2 and ρ_3, respectively. For the range of 80–200 K, $\rho_2 = 0.724$ and $\rho_3 = 0.003$ are found, whereas in the range of 220–320 K, $\rho_2 = 0.233$ and $\rho_3 = 0.021$. The $1/n_{ap} - 1$ vs $q/2$ kT plot's linear nature suggests that the n values might be represented by the voltage deformation of barrier height Gaussian distribution.

The Ga_2O_3 is well-known for having a high breakdown voltage (V_{BD}), making it suited for high-temperature applications. The *I–V* plots are for room temperature between −25 and 5 V to determine the V_{BD} for a 30-nm amorphous Ga_2O_3 thin film. The calculated V_{BD} is 5.6 MV cm^{-1} (Fig. 5). In the literature, for a similar Ga_2O_3 MIS structure, breakdown voltages of 7 MV cm^{-1} have been reported [31]. The resulting relatively low breakdown voltage and remarkable leakage current can be attributed to native oxides between the Ga_2O_3–p-Si interface and attributed to the presence of both Ga interstitial and O vacancies.

The *C–V* and G/ω–*V* measurements conducted at various frequencies between 500 Hz and 1 MHz using an HP 4192A LF impedance analyzer are used to investigate the dielectric behavior and trapping effects of the amorphous Ga_2O_3 layer. The frequency-dependent *C–V* and G/ω–*V* plots of the Au/Ni/Ga_2O_3/p-Si structure at ambient temperature are shown in Fig. 6a and b. The *C–V* plots clearly reveal the typical operating modes of ideal MIS systems, such as inversion, depletion, and accumulation and show similar behavior to a typical MOS capacitor [29,30]. For negative bias voltage less than −3 V, an inversion layer of electrons forms at the interface. Capacitance overshoot at the start of inversion is regularly seen in *C–V* plots and thought to be due to the oxide's trapping centers filling up. With decreasing frequency, the *C–V* plots shift to a more negative gate bias (Fig. 6a). At ambient temperature, the interface traps are closer to the valence band, explaining the horizontal shift. At lower frequencies, more traps are effective in charge build-up; therefore, to compensate for the charge due to interface traps, more negative gate biases are required at lower frequencies for the same band bending in the semiconductor, creating a horizontal shift in the *C–V*. However, for various frequencies, the maximum capacitance values are fairly close to one another, at about 8 nF. Although these frequency-dependent *C–V*

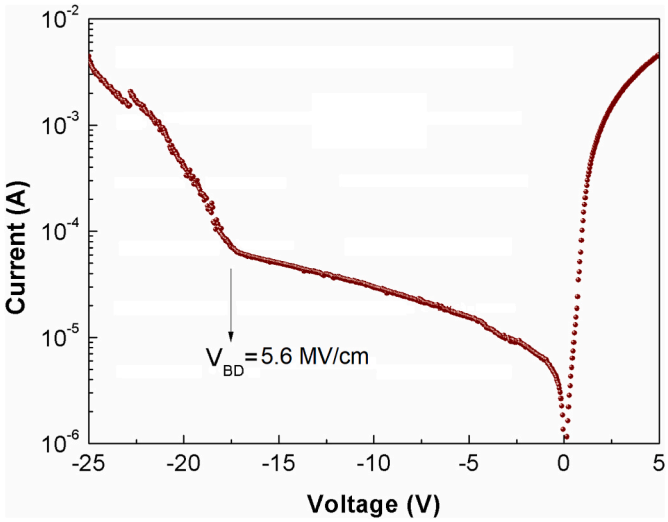

Fig. 5. Semilogarithmic *I–V* curve of the Au/Ni/Ga_2O_3/p-Si structure at room temperature. The breakdown voltage was 5.6 MV cm^{-1}.

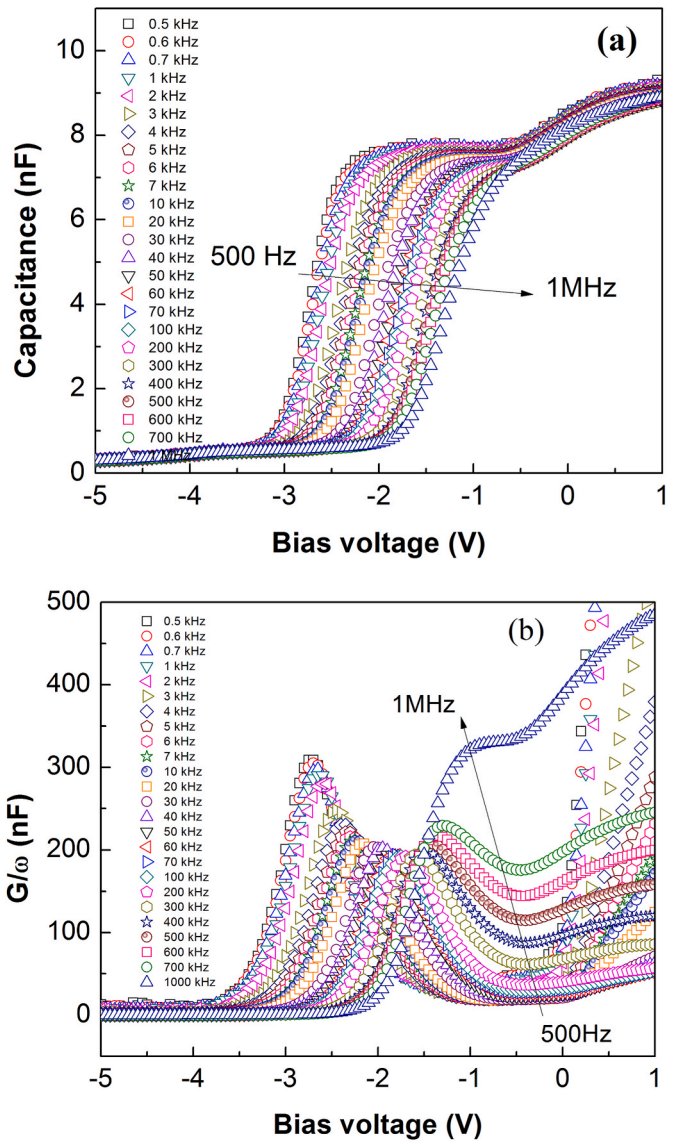

Fig. 6. Measured frequency-dependent (a) *C–V* and (b) *G/ω-V* plots of the Au/Ni/Ga_2O_3/p-Si structure at ambient temperature.

curves are not like those of the MIS stack made of various dielectric alloys, research studies show that MIS structures prepared with Ga_2O_3 show similar frequency-dependent behavior [31]. This unusual behavior shows that the Ga_2O_3 layer formed on p-Si has low interface traps. Otherwise, these interfacial traps can greatly increase their capacitance values at low frequencies because they can easily follow AC signals at these frequencies, resulting in a significant increase in the differential capacitance maximum value between low and high frequencies. The additional kink near −0.5 V is attributed to the interface traps located between p-Si substrate and Ga_2O_3 insulator layers. The nonideal MIS capacitance curve might undergo a parallel shift from the ideal curve because of the flat band voltage, fixed charge, oxide trapped charge, interface trapped charge, and mobile oxide charge effects [31]. The *G/ω–V* plots give a peak for each frequency in the depletion region, and these peak values also shift to more negative bias voltage regions at lower frequencies (Fig. 6b) similar to the shifts seen in the *C–V* plots due to interface traps. In addition, significantly larger frequency dispersion in *C–V* and *G/ω–V* curves are evident in the trend, especially in the accumulation region. The frequency dispersion seen in accumulation might be due to a low-resistance oxide layer next to the interface rather than a large density of interface states at the conduction band edge [32].

The dielectric constants of the Au/Ni/Ga_2O_3/p-Si structure are computed as a function of frequency (500 Hz–1 MHz) using the following formula:

$$\varepsilon' = \frac{C}{C_0} = \frac{Cd}{\varepsilon_0 A} \tag{3}$$

where ε_0 is the vacuum permittivity equal to 8.854×10^{-14} F cm^{-1} and *C*, *d*, and *A* are the measured capacitance, thickness, and area of the specimen, respectively. The imaginary part of the permittivity (ε″) or loss factor and dissipation factor (*tan δ*) are given as follows:

$$\varepsilon'' = \frac{G}{\omega C_0} = \frac{Gd}{\varepsilon_0 A \omega} \tag{4}$$

$$tan\delta = \frac{\varepsilon'}{\varepsilon''} \tag{5}$$

where *G* is the measured conductance and *ω* is the angular frequency. The loss factor is the energy lost in the dielectric due to frictional damping, which prevents the bound charge's displacement from remaining in phase with field changes. The frequency-dependent real (ε′) and imaginary (ε″) parts of the dielectric constant at −1 V and zero bias used to study the dielectric characteristic of the Au/Ni/Ga_2O_3/p-Si structure in the accumulation region are shown in Fig. 7a and b. The dielectric constant has a value of about 9 and does not change much depending on the frequency at zero bias (Fig. 7a). These dielectric values are consistent with previous research [20,31]. Traditional dielectric oxides have a dispersion behavior for ε′. At low frequencies, dielectric materials have large dielectric constant values, which gradually drop as frequency increases. The extrinsic (space charge, grains, and grain borders) and intrinsic (ionic, bipolar, and electronic) contributions to dielectric polarization are responsible for a high dielectric constant at low frequencies. The relaxation of extrinsic variables causes the dielectric constant to decrease with increasing frequency. The Maxwell–Wagner type of interfacial polarization, however, may be responsible for a large dielectric constant at low frequencies [33]. In contrast to the dielectric constant, the dielectric loss factor (Fig. 7b) and *tanδ* (Fig. 7c) initially decrease with increasing frequency, reach a minimum, and then increase again as frequency increases. Actually, the minimum value of ε′ corresponds to the maximum value of ε″. This is known as inductive behavior and is the outcome of series resistance (R_s) and interface traps (D_{it}) interacting with the Au/Ni/Ga_2O_3/p-Si structure [34]. In other words, the sample shows a metallic feature after a certain frequency or voltage value. The *tanδ–f* plots for −1 V and zero bias also exhibit U-shape behavior like the *ε″–f* plots due to the inductive behavior of the structure.

To obtain the energy density distribution profile of interface traps (D_{it}) as well as relaxation time (*τ*) for the Au/Ni/Ga_2O_3/p-Si structure, we use the conductance method due to its higher accuracy and reliability compared to other methods such as surface admittance and high–low frequency capacitance [35]. The conductance method entails measuring *C* and *G/ω* as a function of a number of variables, including DC bias voltage and AC voltage modulation frequency. The value of *Gp/ω* as a function of the frequency of the applied signal is found using Eq. (6) [35,36]:

$$\frac{G_p}{\omega} = \frac{\omega C_{ox}^2 G_m}{\omega^2 (C_{ox} - C_m)^2 + G_m^2} = (qAD_{it}/2\omega\tau) ln\left(1 + \omega^2\tau^2\right) \tag{6}$$

where *ω* is the angular frequency (= 2π*f*), C_{ox} is the capacitance of the interfacial oxide layer, and C_m and G_m are the measured capacitance and conductance, respectively.

The measured C_m and G_m/ω values for varied applied bias voltages are used to generate the *Gp/ω–f* graphs (Fig. 8). These graphs show a peak for each voltage $(Gp/\omega)_{max}$, with the peak location shifting from low to high frequency as the applied bias voltage decreases. The D_{it} is probably responsible for this peak behavior. At the peak values (Fig. 8),

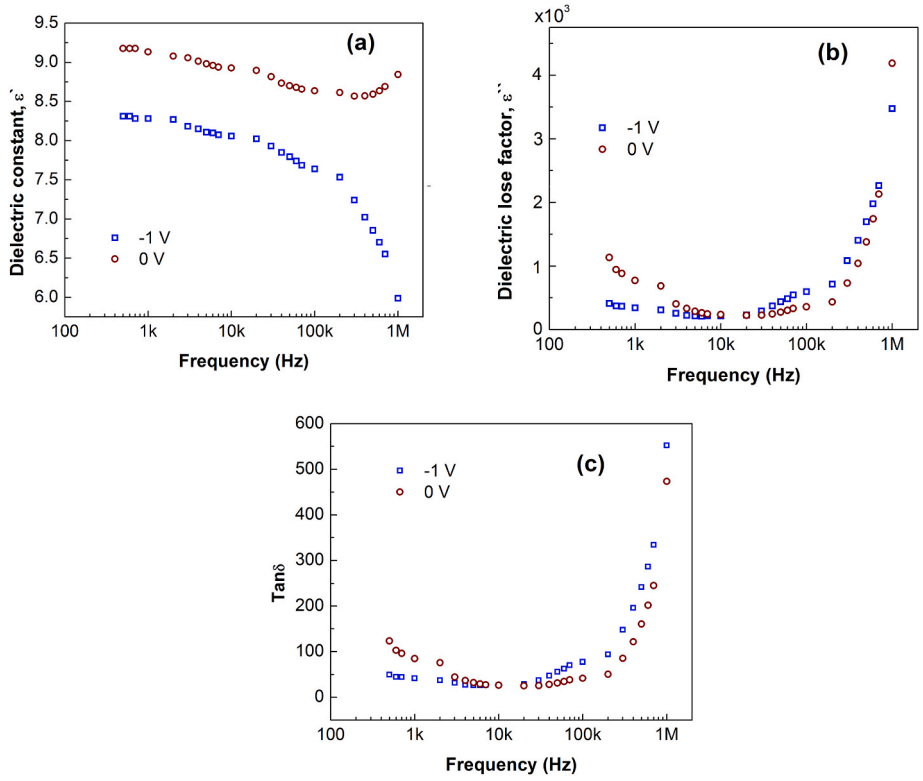

Fig. 7. The (a) e′–*f*, (b) ε″–*f*, and (c) *tanδ*–*f* plots of the Au/Ni/Ga_2O_3/p-Si structure at ambient temperature.

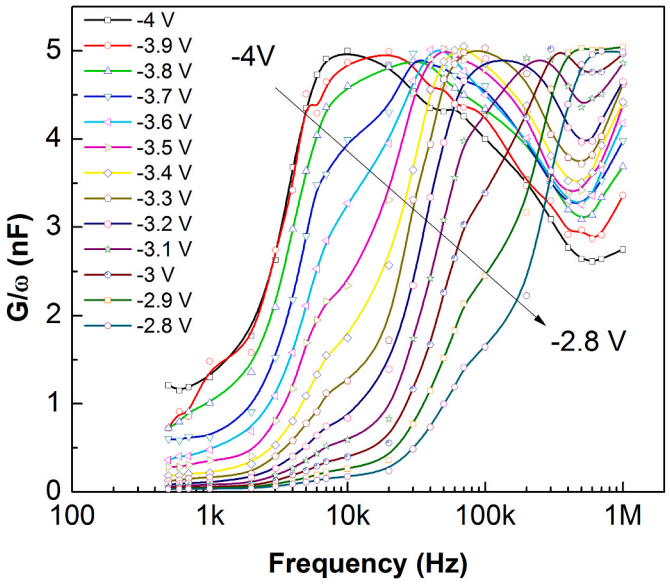

Fig. 8. The *Gp/ω* vs frequency plots at different bias voltages (−4 to −2.8 V with 0.1 V steps) for Au/Ni/Ga_2O_3/p-Si structure.

d(*Gp*/*ω*)/d(*ωτ*) = 0 and this peak condition for Eq. (6) provides *ωτ* = 1.98. The energy of interface traps (E_{it}) in p-type Si may be described as Eq. (7) about the top of the E_V band on the Si surface [29]:

$$E_{it} - E_V = q(\varphi_s + E_F) \tag{7}$$

where *q* is the electronic charge, φ_S is the surface potential, and E_F is the Fermi energy level. The D_{it} values are calculated via multiplying the maximum values $(G_p/\omega)_{max}$ by 2.5 [$D_{it} \approx \frac{2.5}{Aq}(G_p/\omega)_{max}$] and interface states relaxation time is estimated by $\tau \approx 1.98/\omega_p$ [36]. The extracted D_{it} and its *τ* values as a function of energy separation from the valence band edge are shown in Fig. 9. The values of D_{it} are 2.43×10^{12} to 2.50×10^{12} $eV^{-1}cm^{-2}$ and are almost constant with energy (Fig. 9). The manufacturing of the gate dielectric and device passivation applications is well suited to such low D_{it} values. In addition, from the midgap to the band edges, the interface trapped charge lifetime varied from 0.45×10^{-6} to 31.52×10^{-6} s. These results demonstrate that, at frequencies greater than 1 MHz, the interface charges at traps cannot easily keep pace with the AC signal.

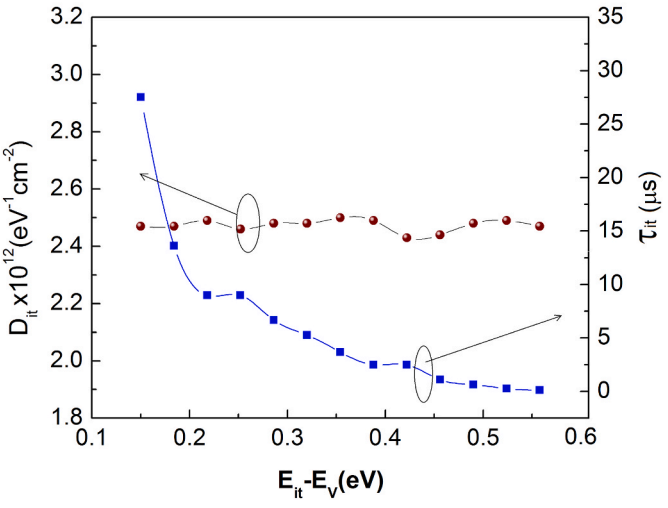

Fig. 9. The conductance technique was used to obtain D_{it} and *τ* as a function of energy.

4. Summary and conclusion

PEALD was used to deposit highly smooth and low-defect-density amorphous Ga_2O_3 thin films as dielectric gates for electronic device applications. The XPS depth-profiling analysis showed that the ratio of Ga/O was 0.8, quite close to the ideal ratio of 2/3 (0.67). The temperature-dependent *I–V* and frequency-dependent (500 Hz–1 MHz) *C–V* and G/ω–*V* characteristics of the Au/Ni/Ga_2O_3/p-Si structure were studied for the electrical and dielectric behaviors of the amorphous Ga_2O_3 thin films. The barrier inhomogeneity examined using temperature-dependent *I–V* showed that the barrier formed by the Ga_2O_3 layer was homogeneous due to a smaller value of σ_0 and, therefore, exhibited an effective passivation feature. The *C–V* plots shifted to a more negative gate bias with decreasing frequency due to interface traps being closer to the valence band at ambient temperature. However, for various frequencies, the maximum capacitance values were close to one another, at about 8 nF. The G/ω–*V* plots showed a peak for each frequency in the depletion region, and these peak values also shifted to more negative bias voltage regions at lower frequencies similar to the shifts seen in the *C–V* plots due to interface traps. Regardless of the applied frequency, Ga_2O_3 thin films exhibited a good dielectric constant of ~9 at zero bias voltage. Moreover, at the Ga_2O_3–p-Si interface, thorough *C–V* analysis revealed low state densities of the order of 10^{12} $eV^{-1}cm^{-2}$, which is within the acceptable range of an electronic device. Therefore, our experimental results indicate their usefulness for several dielectric gate and device passivation applications.

Prime novelty statement

The prime novelty of this research is the structural, electrical and dielectric properties of the Ga_2O_3 thin film obtained by the plasma-enhanced atomic layer deposition (PEALD) were investigated in detail. The charge-transport mechanisms of this structure were studied using temperature-dependent current-voltage (*I–V*) characteristics. The dielectric behavior of the fabricated MOS structure was explored using frequency-dependent capacitance-voltage (*C–V*) and conductance-voltage ($G/\omega-V$) experiments. To better understand the characteristics of the Ga_2O_3/p-Si interfaces, the interface trap density (D_{it}) was estimated using the admittance spectroscopy method.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The authors do not have permission to share data.

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